Preliminary Results of Tests on TRD Front End Prototype Chip

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- Introductory Remarks
- Test Conditions
- DC Tests
- Gain and Pulse Shaping Function
- Fast Overload Recovery Function
- Logic Function
- Test Generator Function
- Next Steps

INTRODUCTORY REMARKS

- The main purpose of my presentation is to show results of the preliminary tests on a HCR-TRD front end prototype chip.
- ASIC test needs an appropriate infrastructure.

It was designed, built and tested:

- PCB – as chip mounting/bonding base
- Test Board – for electronic tests of the chip
- Mother Board – for testing the chip as HCR-TRD FEE

TB and MB contain the following blocks:

- power supplies
- adjustable voltage references
- digital (logic) interface (between chip and DAQ)
- analog interface (buffers)

HCR-TRD ASIC Test Board

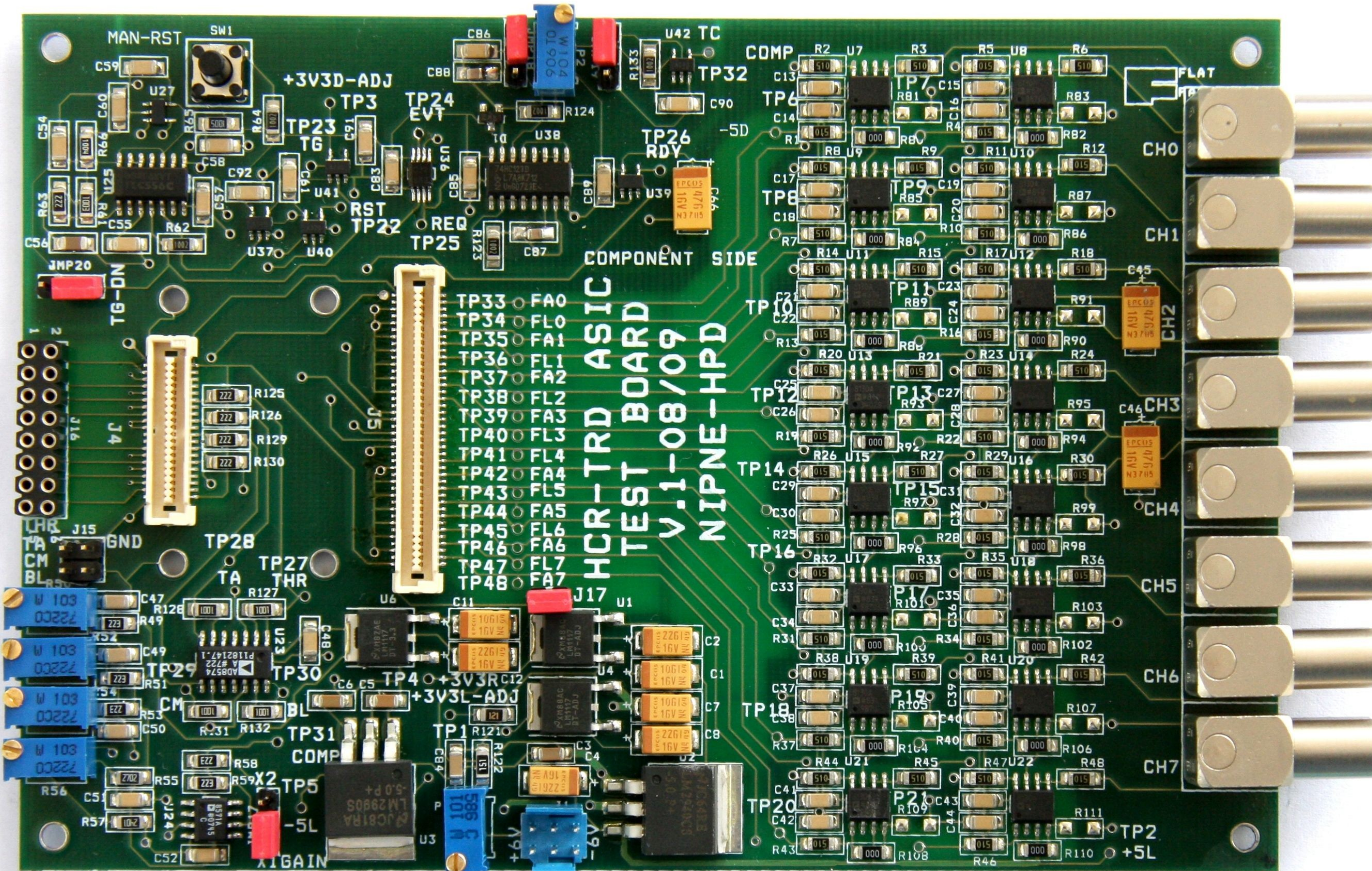


FIG. 3

TEST CONDITIONS

Unless otherwise specified:

- Setup:
  - Pulse Generator HP8004A ($T_R \approx 0.8$ ns)
  - Digital Oscilloscope DPO 4104 (BW = 1GHz, SR = 5 GS/s)
  - Digital Multimeter HP 34401A (6 digits)
  - NIM Standard Power Supply (+/- 6VDC)
- Chip settings:
  - power supply = 3.3 V
  - baseline level = 500 mV
  - common reference = 1 V
  - threshold level = 100 mV
  - shaping time = 40 ns

DC TESTS

⇨ Variation of quiescent supply current vs. operating voltage:

Operating voltage	3.0	3.3	3.6	V
Quiescent current	29.68	30.32	30.71	mA

$\Delta I \approx 1$ mA

Predicted power consumption:
11mW/(analog ch.)
Measured:
12.5 mV/(analog ch. + logic circuitry)

⇨ Baseline level adjustment: 0.2 → 1.0 V (design specification)

⇨ Variation of baseline vs. leakage current injected at the input of the chip:

Fast out

Ch. no.	Leakage current			Δ	
	- 50 nA	0	+ 50 nA		
0	492.0	492.49	492.87	0.87	mV
7	494.38	494.7	494.89	0.51	mV

Design specification: 0.50 mV

Ch. no.	Leakage current			Δ	
	- 50 nA	0	+ 50 nA		
0	497.8	498.34	498.65	0.85	mV
7	493.92	494.33	494.46	0.54	mV

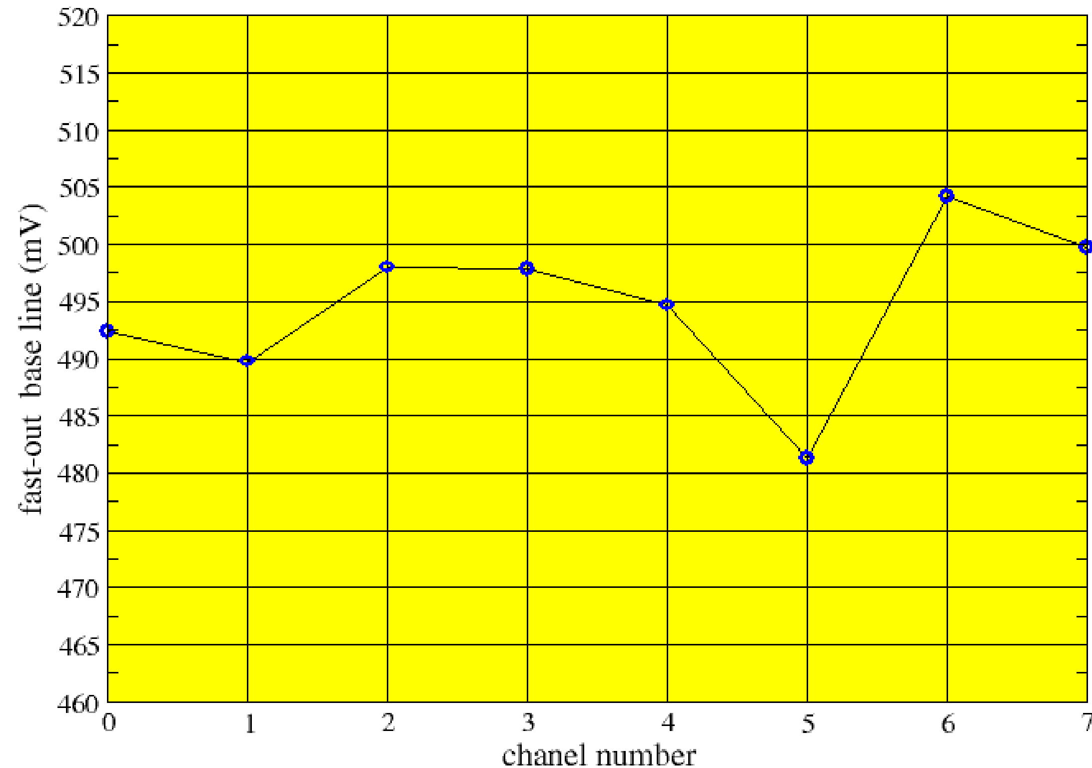
Peak sense out

Variation of baseline vs. channel no. and vs. power supply:

Ch. no.	Power supply			Δ	
	3.0 V	3.3 V	3.6 V		
0	492.74	492.37	492.36	0.38	mV
1	489.93	489.70	189.67	0.26	
2	498.23	497.93	497.88	0.35	
3	498.17	497.87	497.75	0.42	
4	499.93	499.68	499.65	0.28	
5	504.55	504.20	504.19	0.36	
6	481.45	481.27	481.29	0.16	
7	494.86	494.62	494.51	0.35	

Fast out

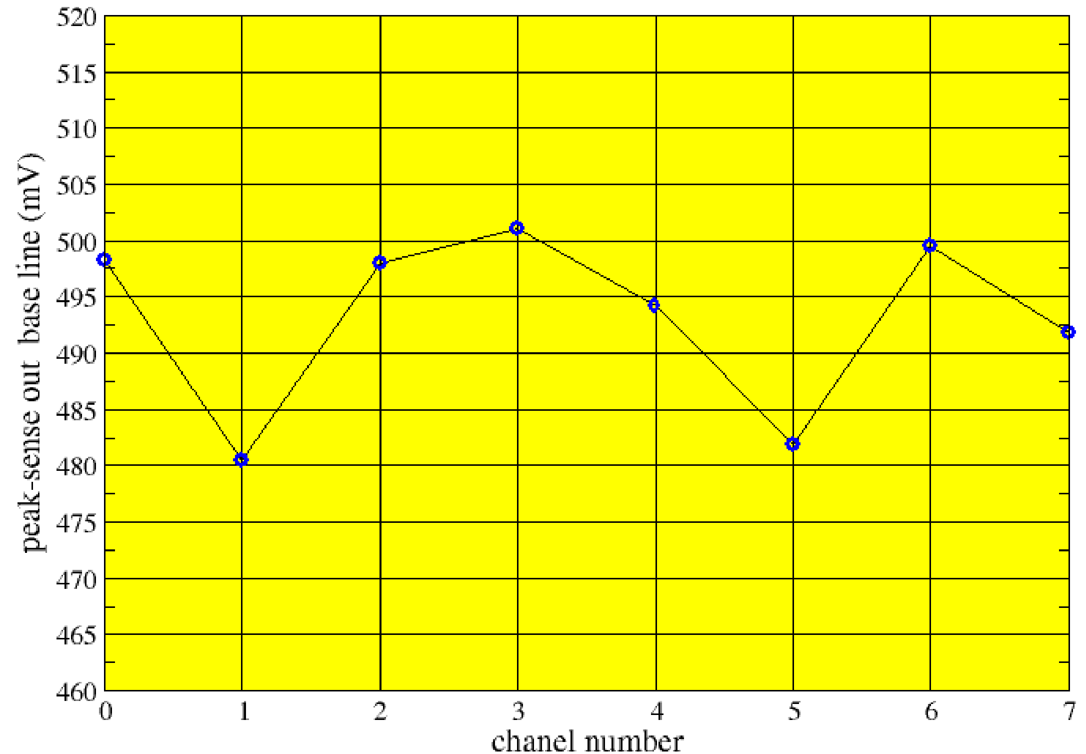
Predicted: 0.35mV



Variation of baseline vs. channel no. and vs. power supply:

Ch. no.	Power supply			Δ	
	3.0 V	3.3 V	3.6 V		
0	498.89	498.30	497.87	1.02	mV
1	480.75	480.41	480.25	0.50	
2	498.58	497.95	497.62	0.96	
3	501.82	501.13	500.74	1.08	
4	491.99	491.81	491.89	0.10	
5	499.92	499.51	499.34	0.58	
6	482.04	481.81	481.82	0.22	
7	494.52	494.24	494.09	0.43	

Peak sense out



GAIN and PULSE SHAPING FUNCTION

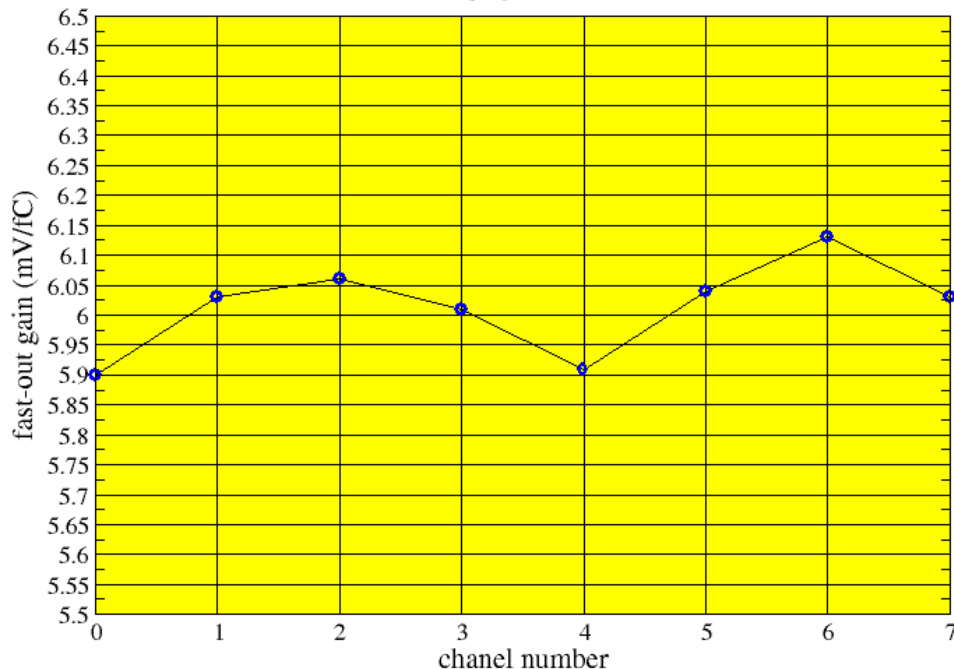
- Conversion gain vs. channel no. and vs. shaping:

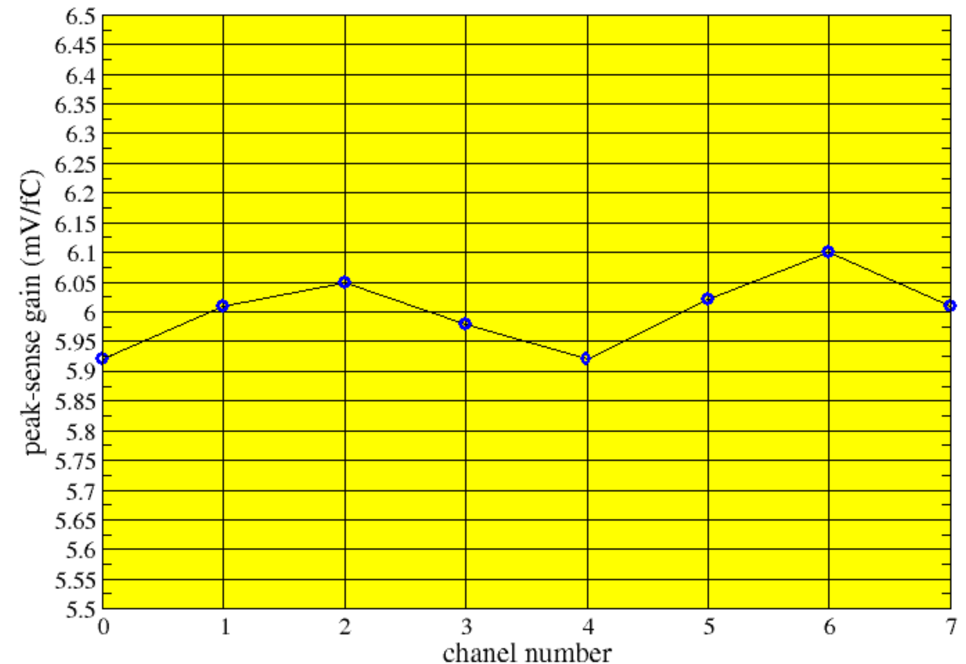
  conversion gain = output voltage signal / input charge signal

  Q_{inj} = 165 fC C_{inj} = 2.13 pF, C_{GND} ≈ 10 pF

ch. no.	0	1	2	3	4	5	6	7	
Fast out	5,90	6,03	6,06	6,01	6,03	6,13	6,04	5,91	mV/fC
Peak sense out	5,92	6,01	6,05	5,98	6,01	6,10	6,02	5,92	

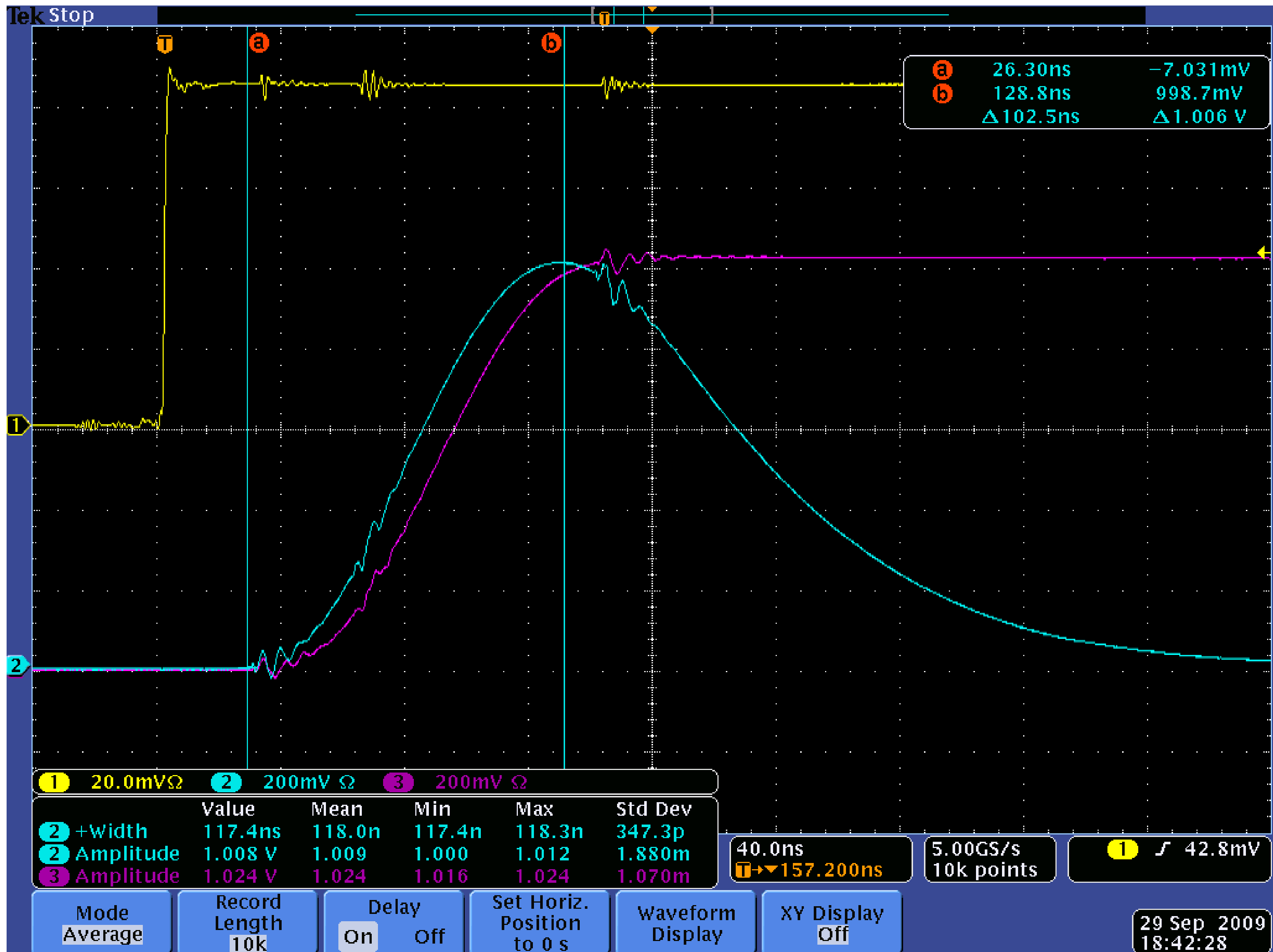
Predicted:
6.10 mV/fC



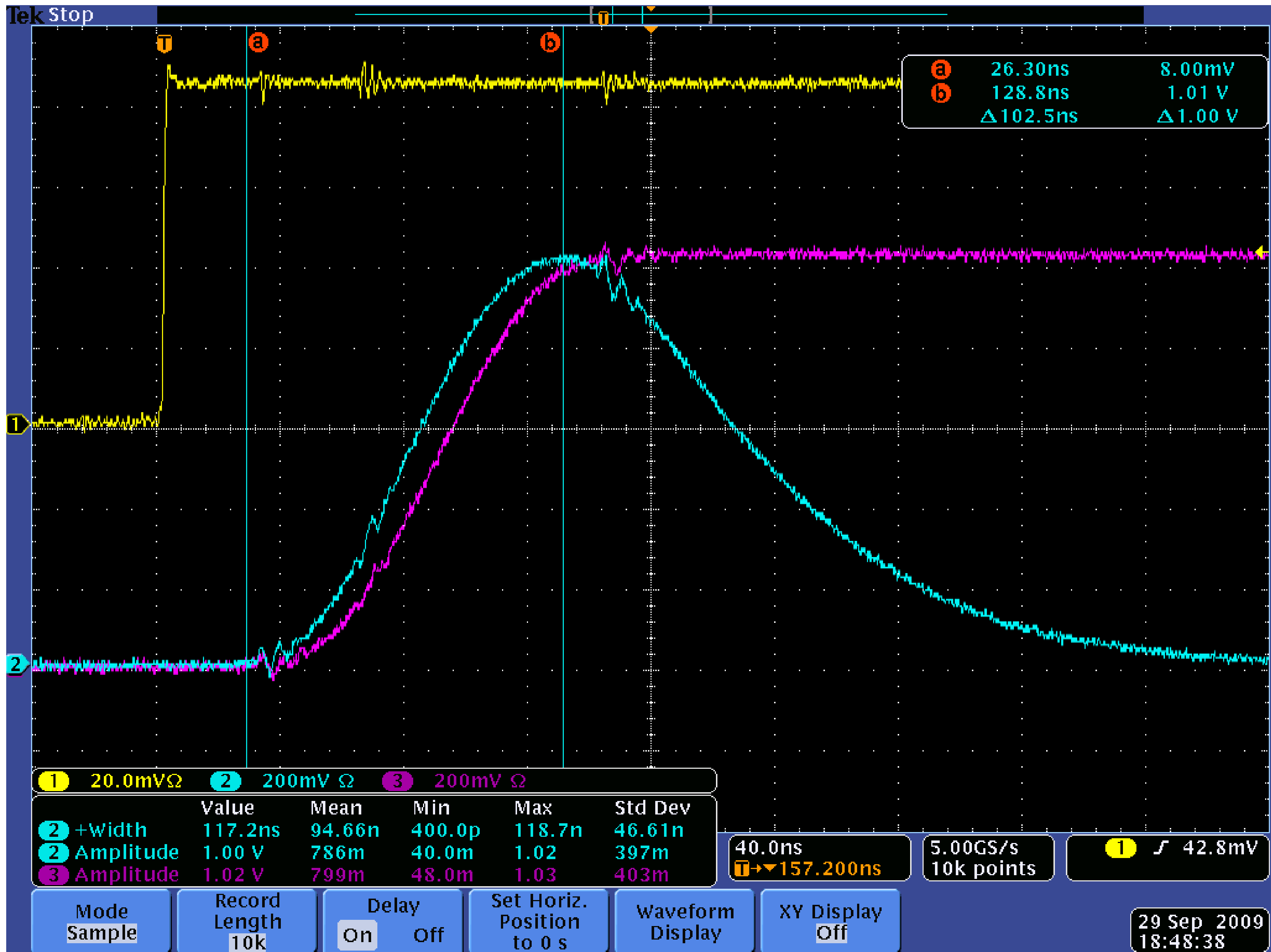


Pulse Shaping

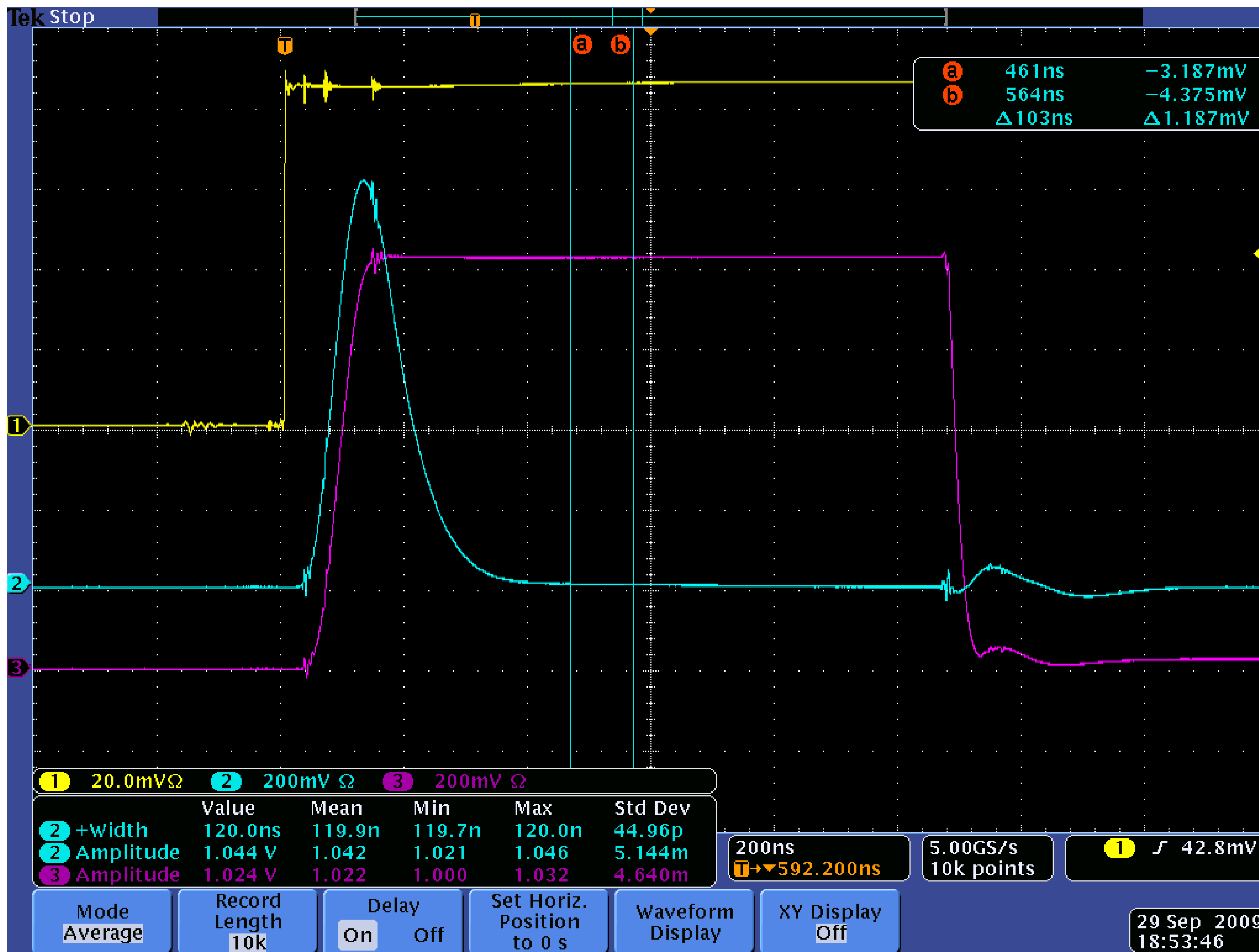
Fast out and peak sense out – details (avg.)



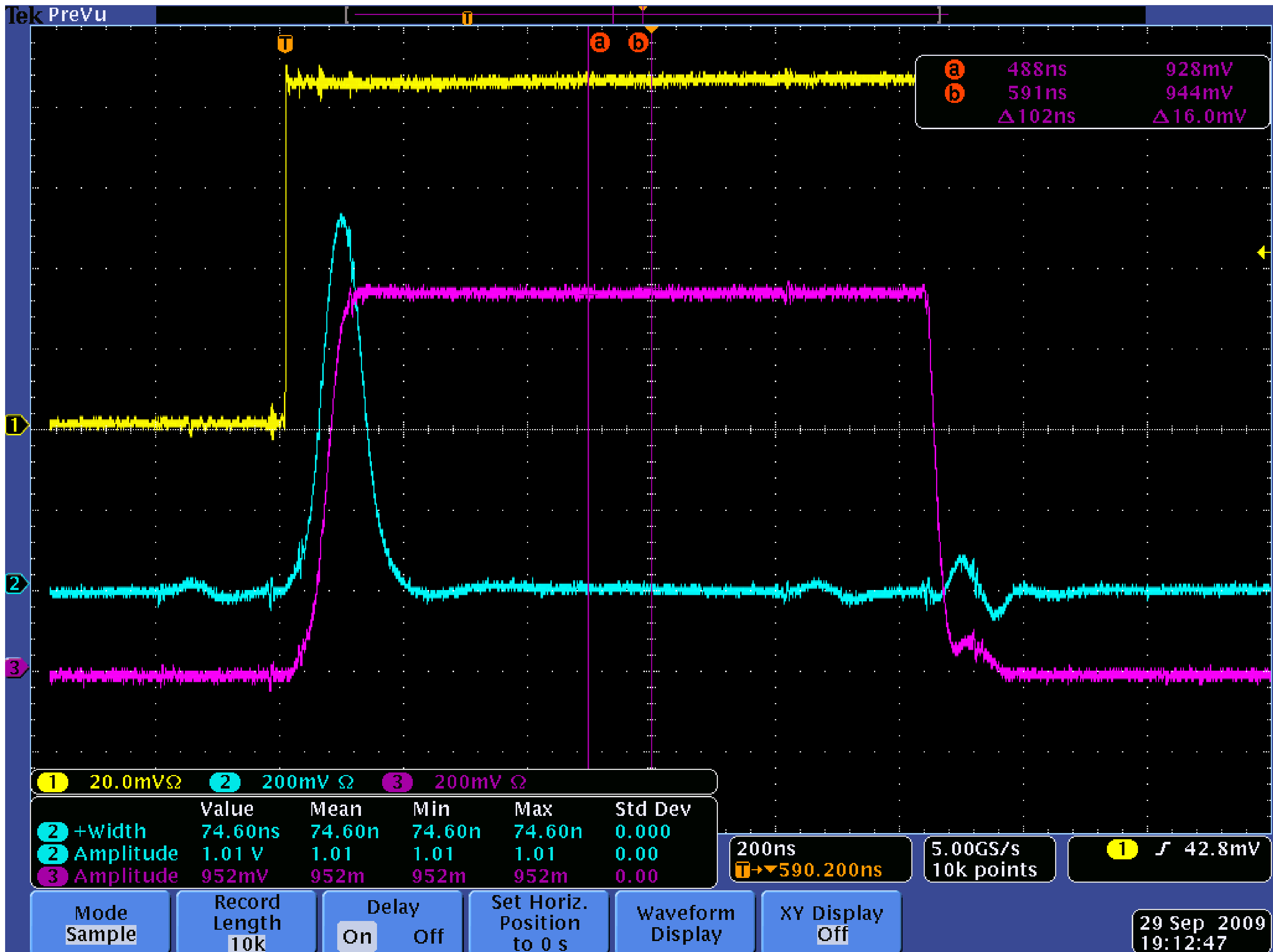
Fast out and peak sense out – details (with noise)



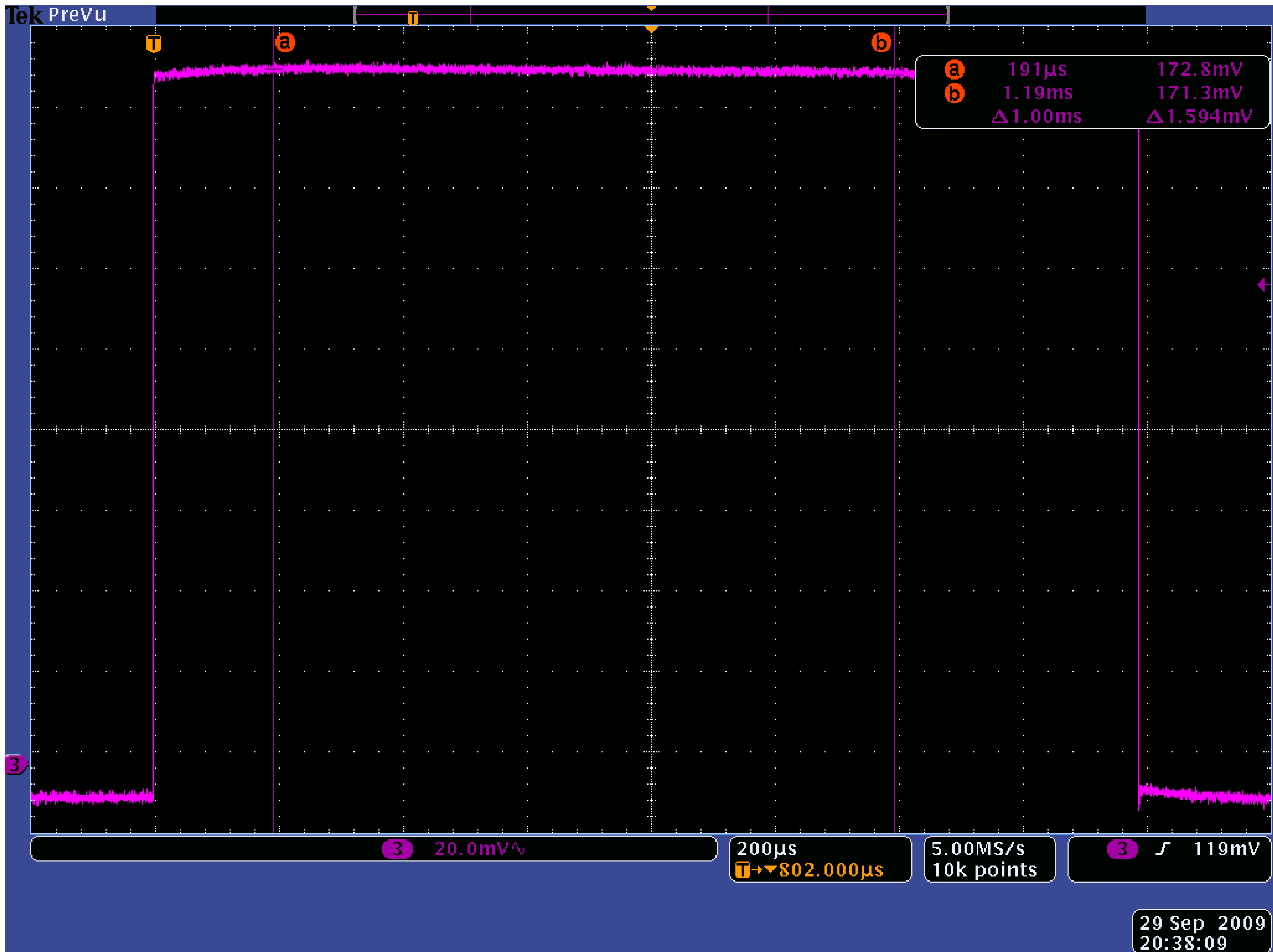
Fast out and peak sense out – complete shapes



Fast out and peak sense out – 20 ns shaping time



Peak sense out – decay slope



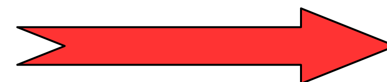
Summary:

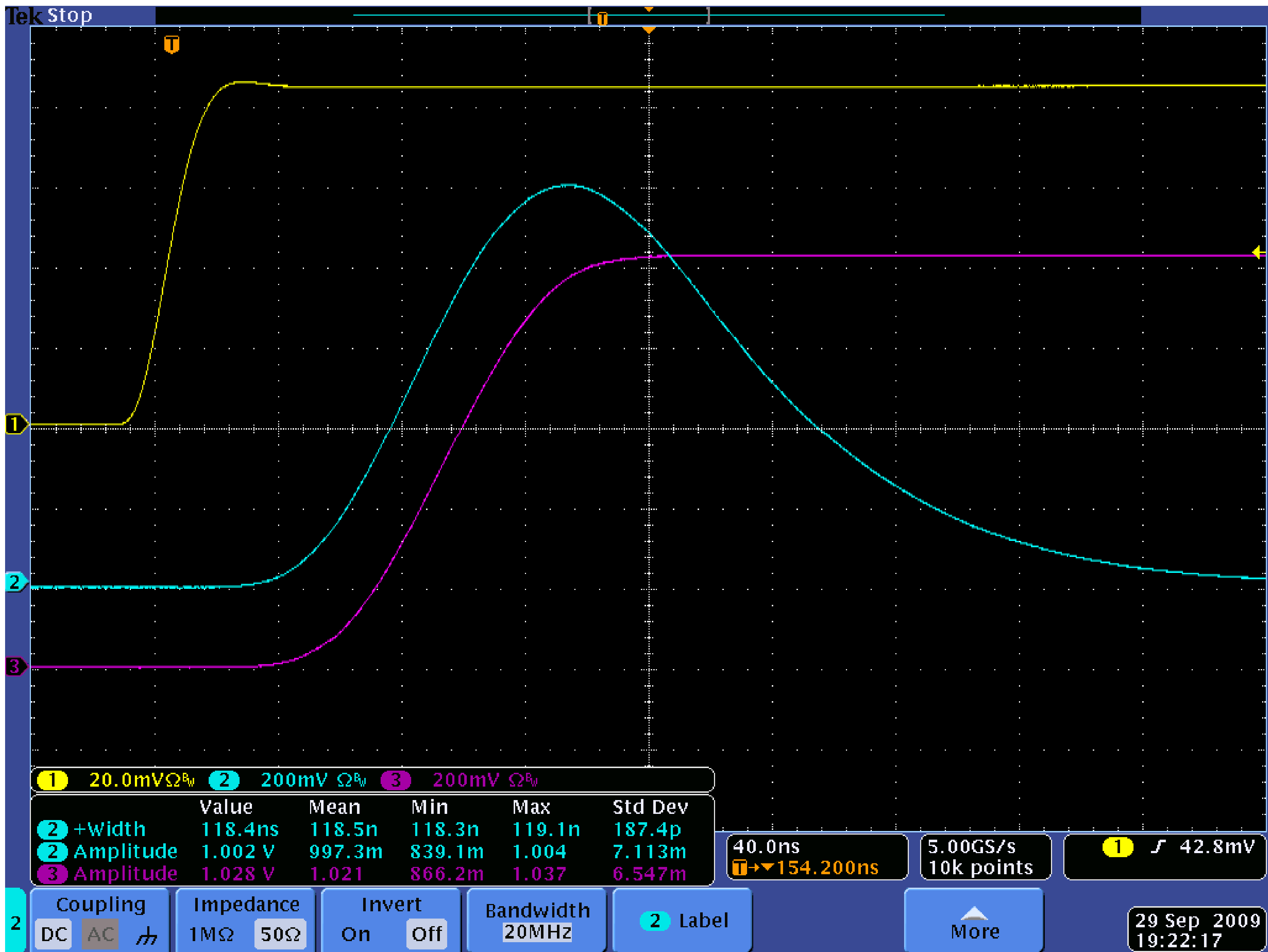
- Spikes were observed at:
  - threshold level
  - peak detection
  - RDY command (peak sense pulse discharge)

  → grounding problems?
  → coupling problems?
  (detailed tests will find their origin)

- Fast output:
  - FWHM time = 118 ns / 110 ns predicted value
  - time to peak = 102 ns

- Flat top:
  - decay ≈ 20 μV/μs / 25 μV/μs predicted

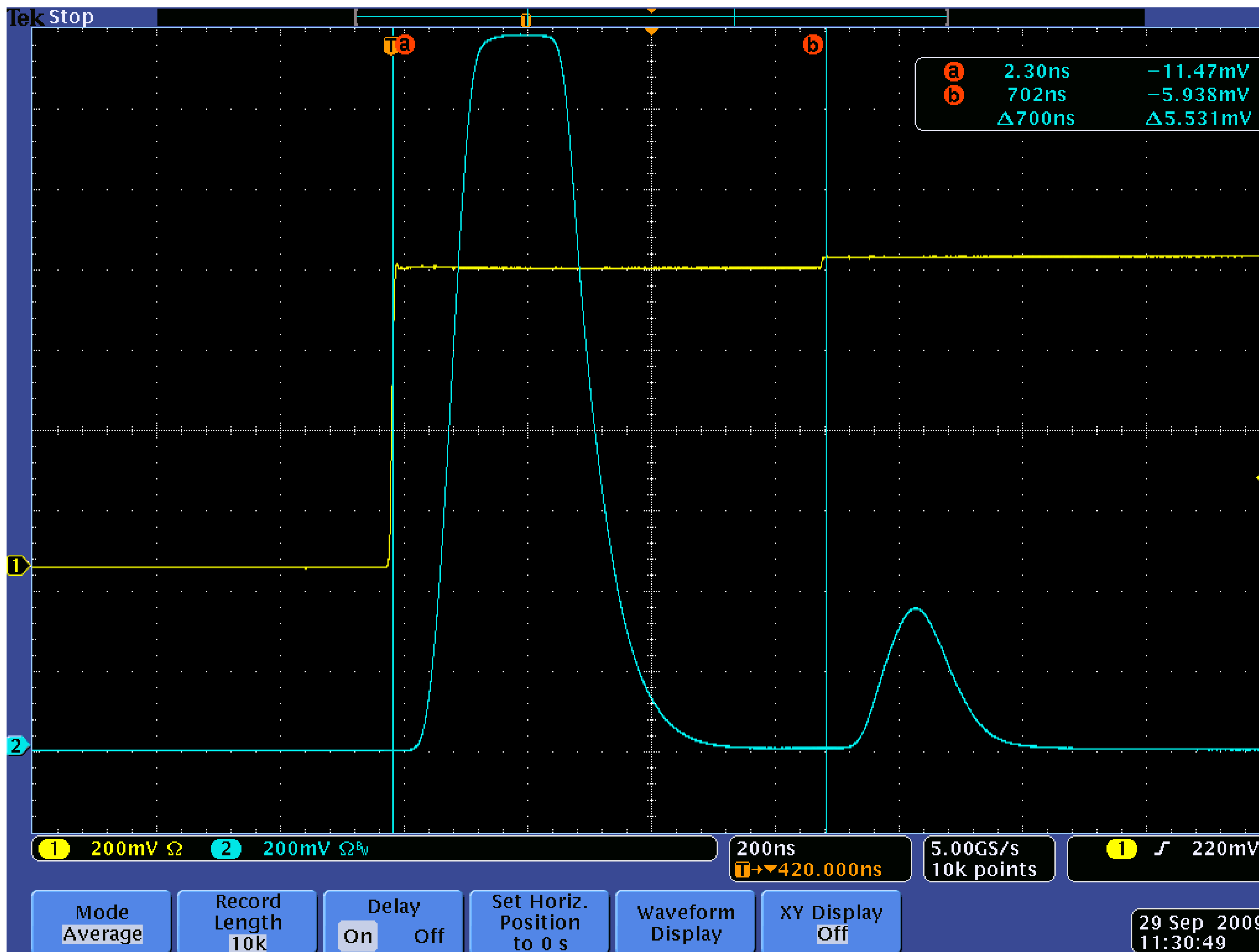
What we hope 



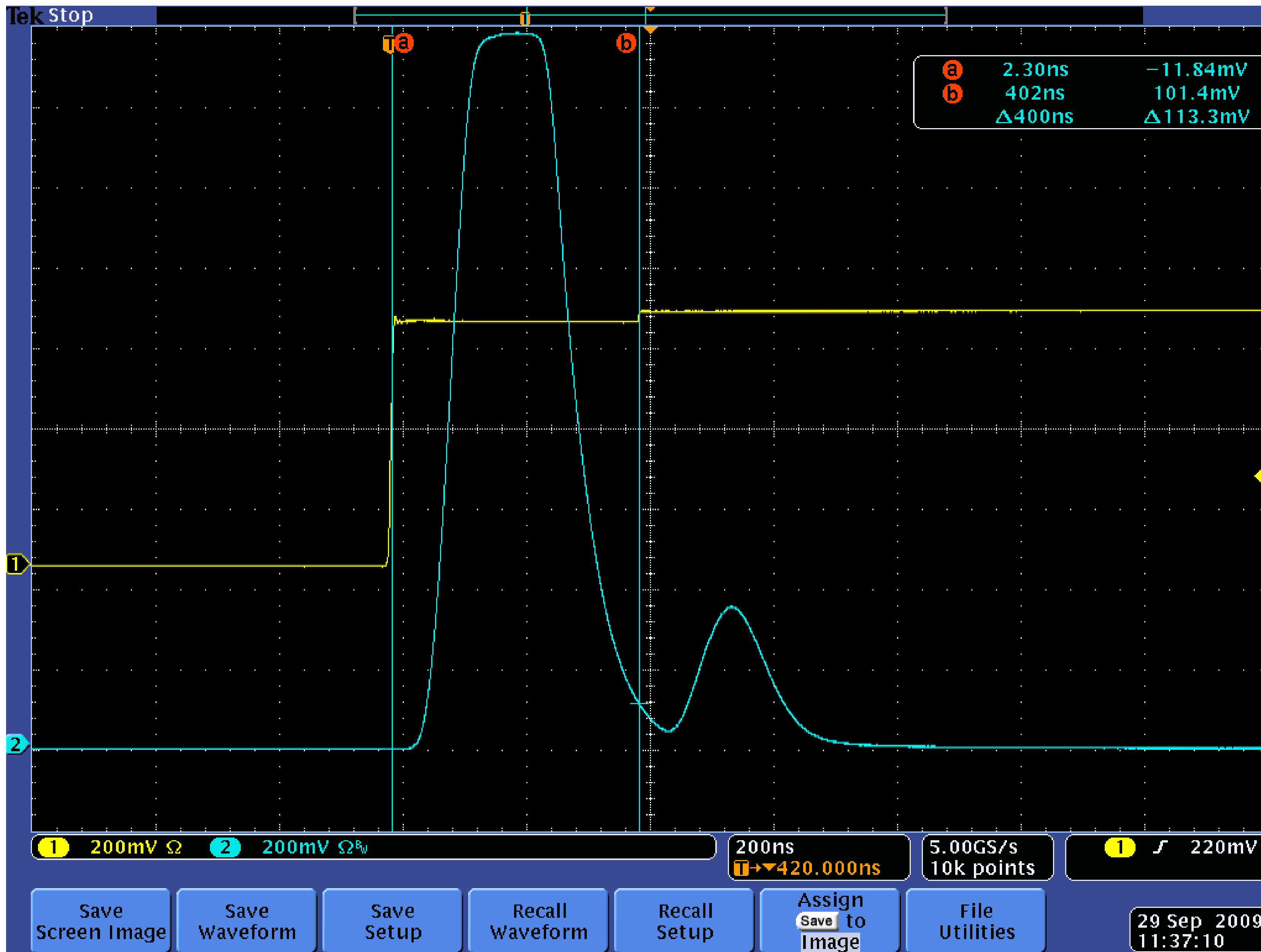
We hope to obtain above shapes ... for larger bandwidth than 20 MHz!

FAST OVERLOAD RECOVERY FUNCTION

- Purpose: to permit correct processing of a signal at shortest time after a strong overloaded pulse
- Level of overloading: x10 full amplitude range (1.65 pC)



700 ns delay between pulses



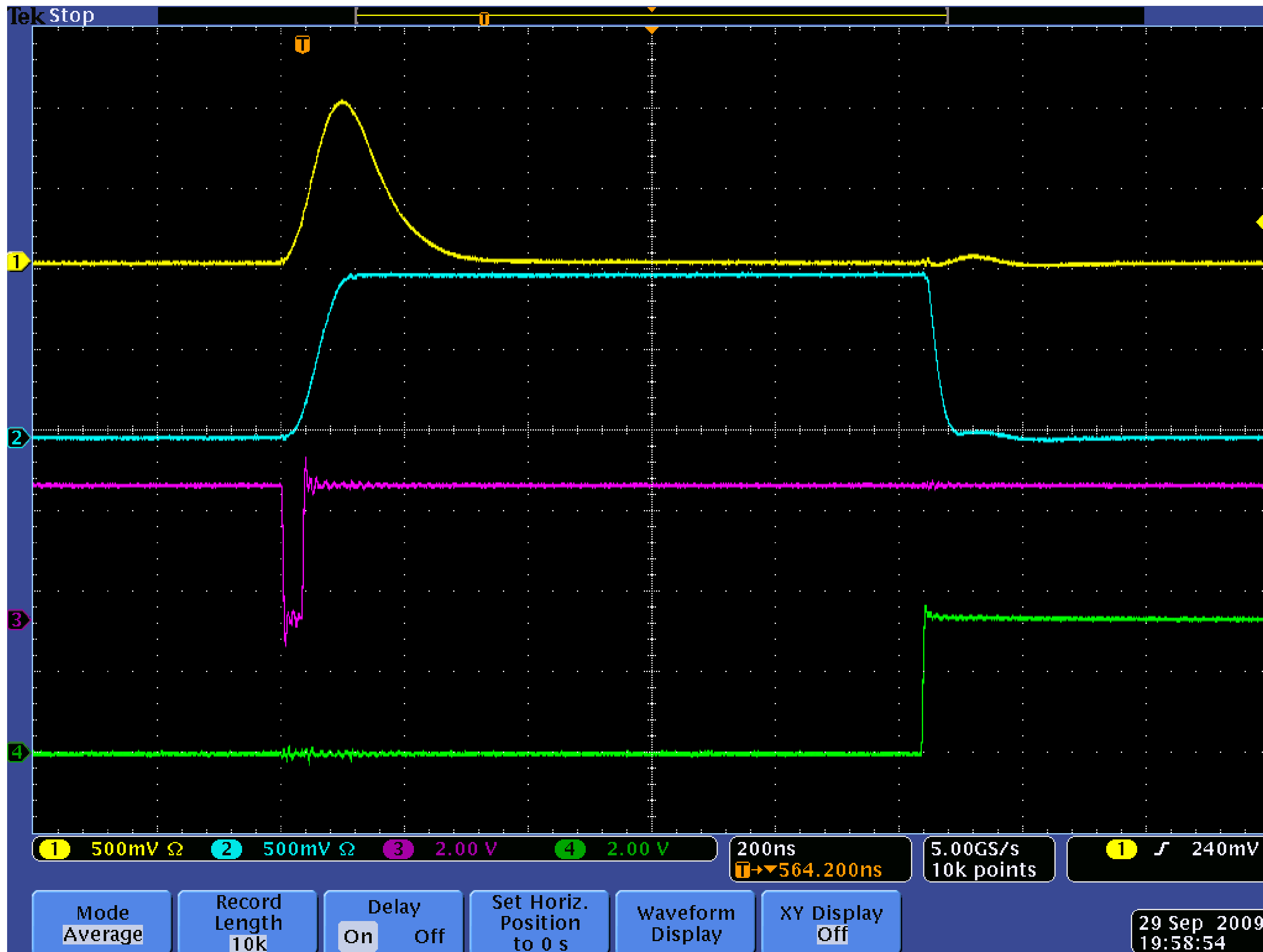
400 ns delay between pulses

Excellent action of fast recovery circuitry!

Design specification: over 300 Kcps

LOGIC FUNCTION

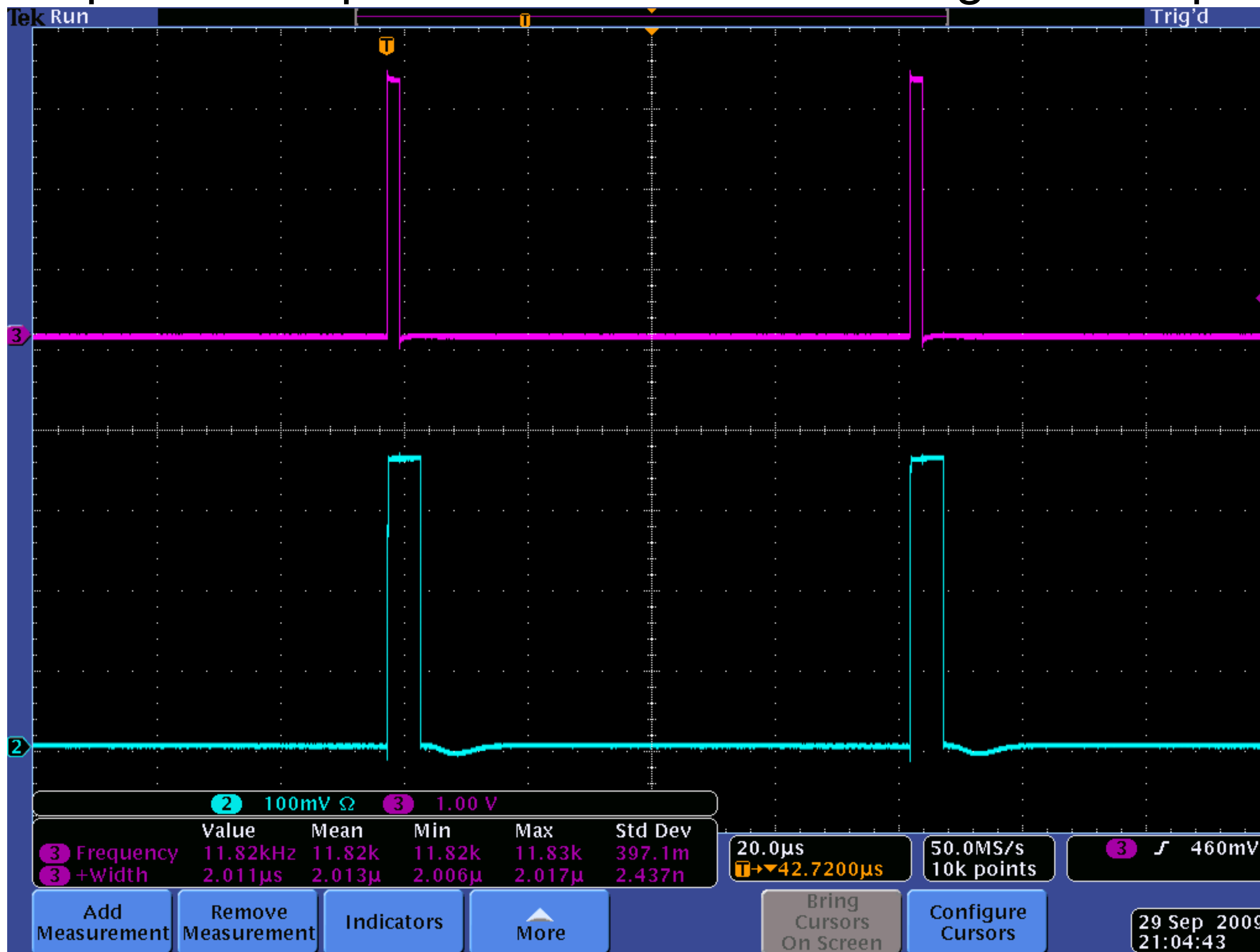
- Logic sequence:
  - EVT signal
  - RDY signal (the end of REQ signal)



TEST GENERATOR FUNCTION

- Function: to test the functionality of signal channels
- Controls: - external triggering (test board, mother board)
  - external reference for amplitude (test board, mother board)

Response of a peak sense channel to the generator pulses



NEXT STEPS

- The presented results were obtained only on one CHIP.
  50 chips were produced (8 are bonded).

- Next steps
  - complete and accurate electronic tests
  - chip tests on HCR-TRD prototypes
  - diagnosis
    - an improved ASIC,test and mother boards

      or
  - an improved version of the chip
    – if it will be necessary!

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