Analog Chip for High Counting Rate Transition Radiation Detector

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Summary

1. Introduction: The first chip for high counting rate (HCR) Transition Radiation Detector (TRD) designed at NIPNE. Goal
2. Specification of the NIPNE first version analog chip for HCR - TRD
3. Some new features, specific to a fast self triggered analog channel, implemented into the chip
4. Additional circuits implemented into the chip
5. Main results
6. Layout of the chip
7. Conclusions

1. Introduction

- the chip is developed in AMS CMOS 0.35μm technology

- acts as an analog, self triggered front end signal processor for HCR-TRD

Goals:

- for testing the new HCR TRDs

- for evaluating different solutions for the HCR TRD front end electronics

2. Specifications of the NIPNE first version analog chip for HCR TRD

- Number of analog channel: 8
- Analog channel outputs:

  a) fast semi-Gaussian output signal

  b) peak-sense output signal
- In chip pulse generator for testing analog channels
- Channel self triggered capability
- Input/Output interface on request/grant basis

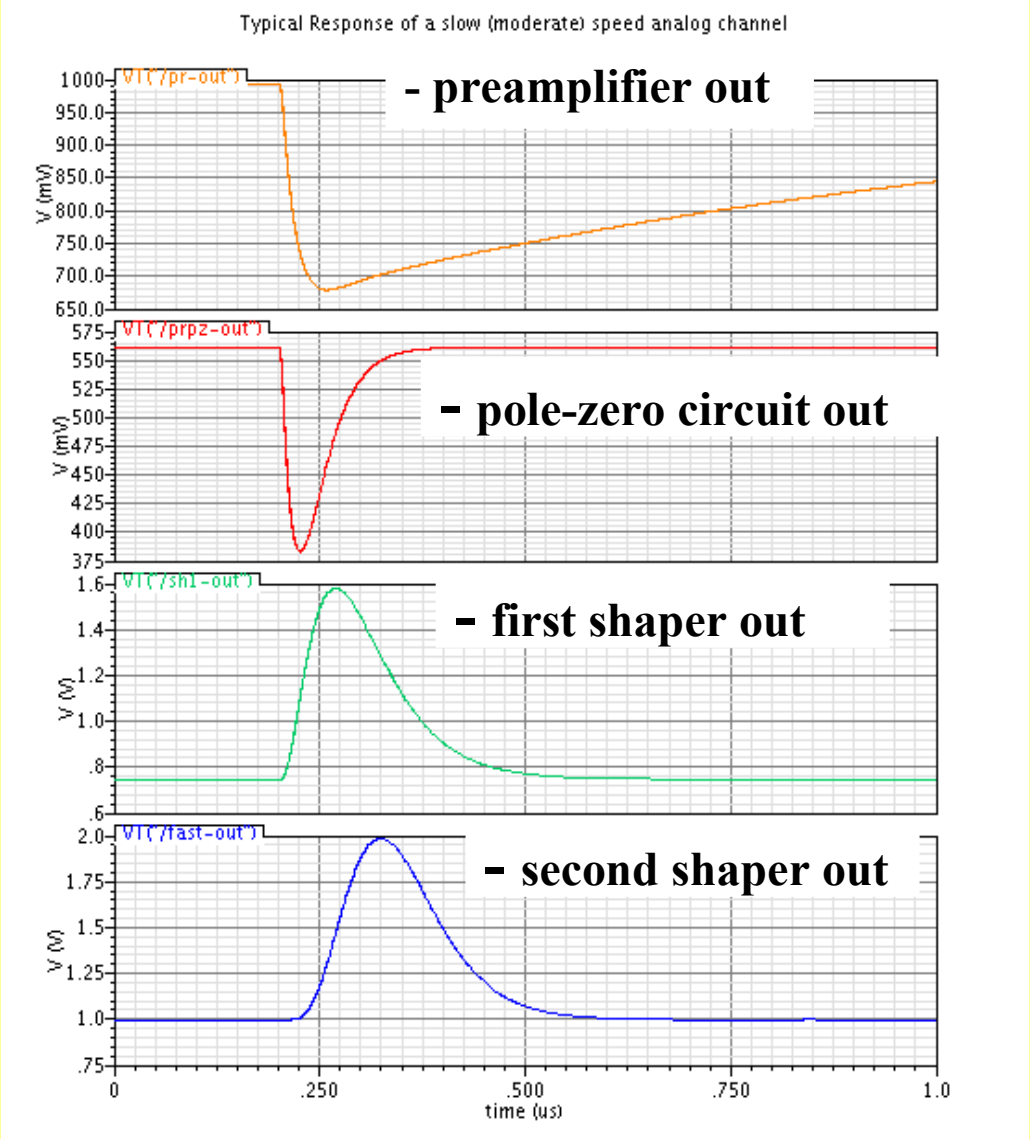
2.1 ASIC analog channels, main specifications

- Average pulse rate: over 300 kcps
- Detector capacitance: 25 pF
- Input range: 0.15fC...165fC
- Input type: DC single ended
- Channel gain: 6.1 mV/fC
- Shaping time: 20 ns or 40 ns (1 bit select)
- Output pulse FWHM: 62 ns or 110 ns
- Output type: single ended
- Output voltage swing 0.....1V
- Output DC voltage level: 0.2V.....1V (cont. adj)
- Output pulse variations:
  - -with Temp=0°.....70° C <0.03%/°C
  - -with Vd=3.0.....3.6V < 0.18%/V
- Output baseline shift:
  - -with Temp=0°.....70° C < 8µV/ °C
  - -with Vd=3.0.....3.6V < 0.07%
  - -with leakage current < 5µV/nA

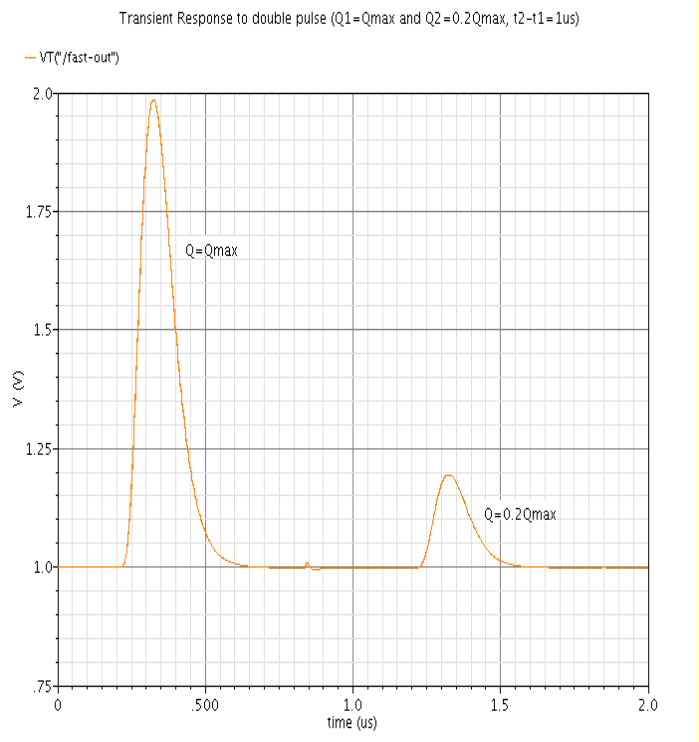
- Channel ENC (Cdet=25pF):
  - -for shaping time 40 ns 980 e
  - -for shaping time 20 ns 1170 e
- Integral nonlinearity:
  - -for shaping time 40 ns < 0.21%
  - -for shaping time 20 ns < 0.9%
- Overshoot (undershoot)
  - - for shaping time 40 ns < 0.2%
  - -for shaping time 20 ns < 0.8%
- Peak-sense out settling time 0.1% <450 ns
- Peak sense out decay < 25µV/µs
- Self triggered capability
  - -threshold variable (cont. adj.): 0.....165 fC (full range)
  - -hit occurence signal logic level
- Power consumption: 11mW/channel

3. Some new features, specific to a fast analog channel, implemented into the chip

3.1 Typical response of analog channel to slow or moderate counting rate



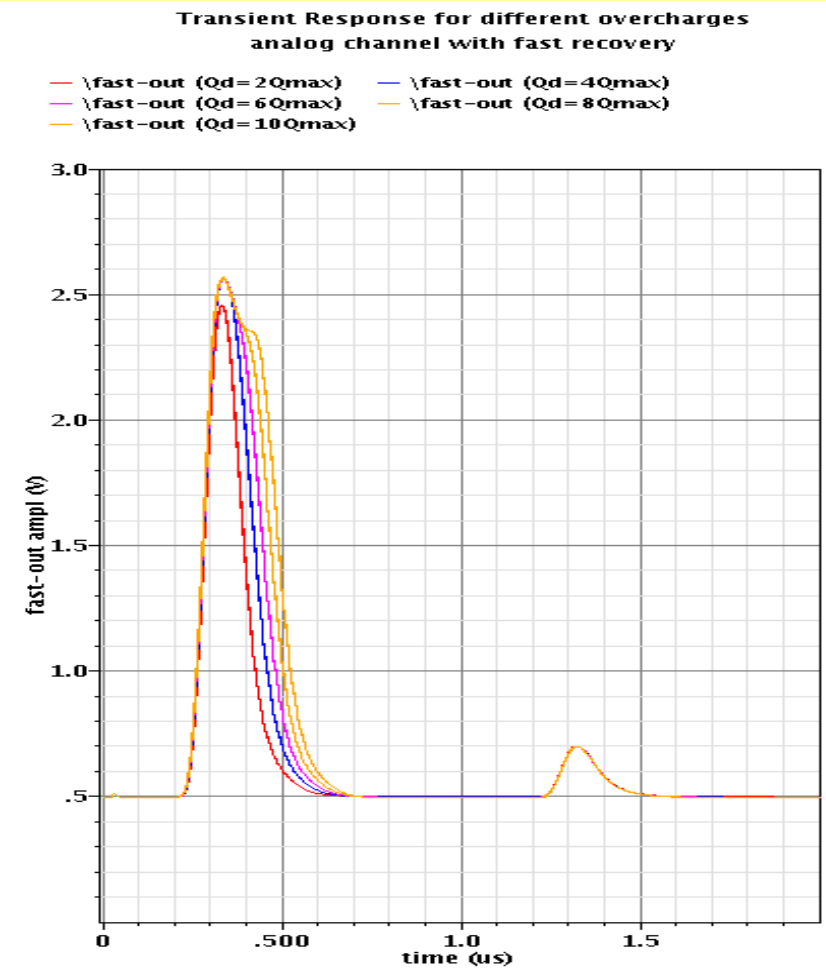
3.2 Good response to double pulse and high rate



- Analog channel output to double pulse
- first pulse of maximum amplitude
- second pulse of 20% of maximum amplitude
- delay between pulses: 1µsec

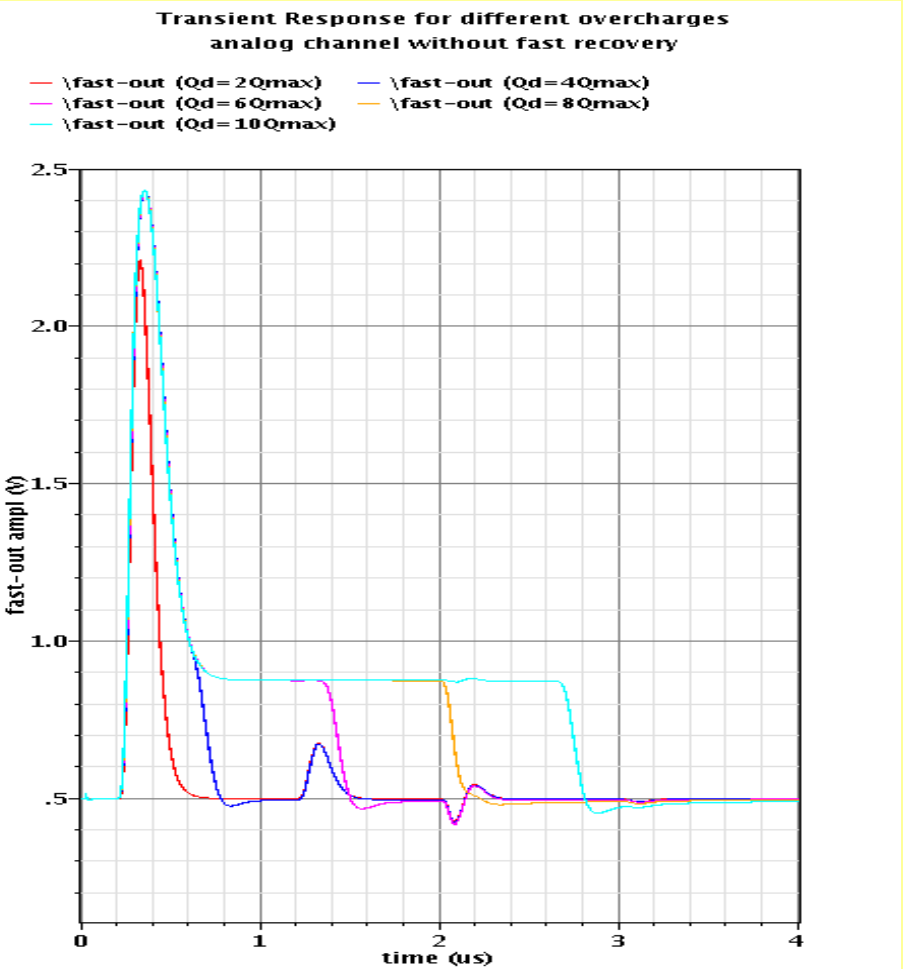
3.3 Fast recovery to charge overload

Channel response with fast recovery circuits:



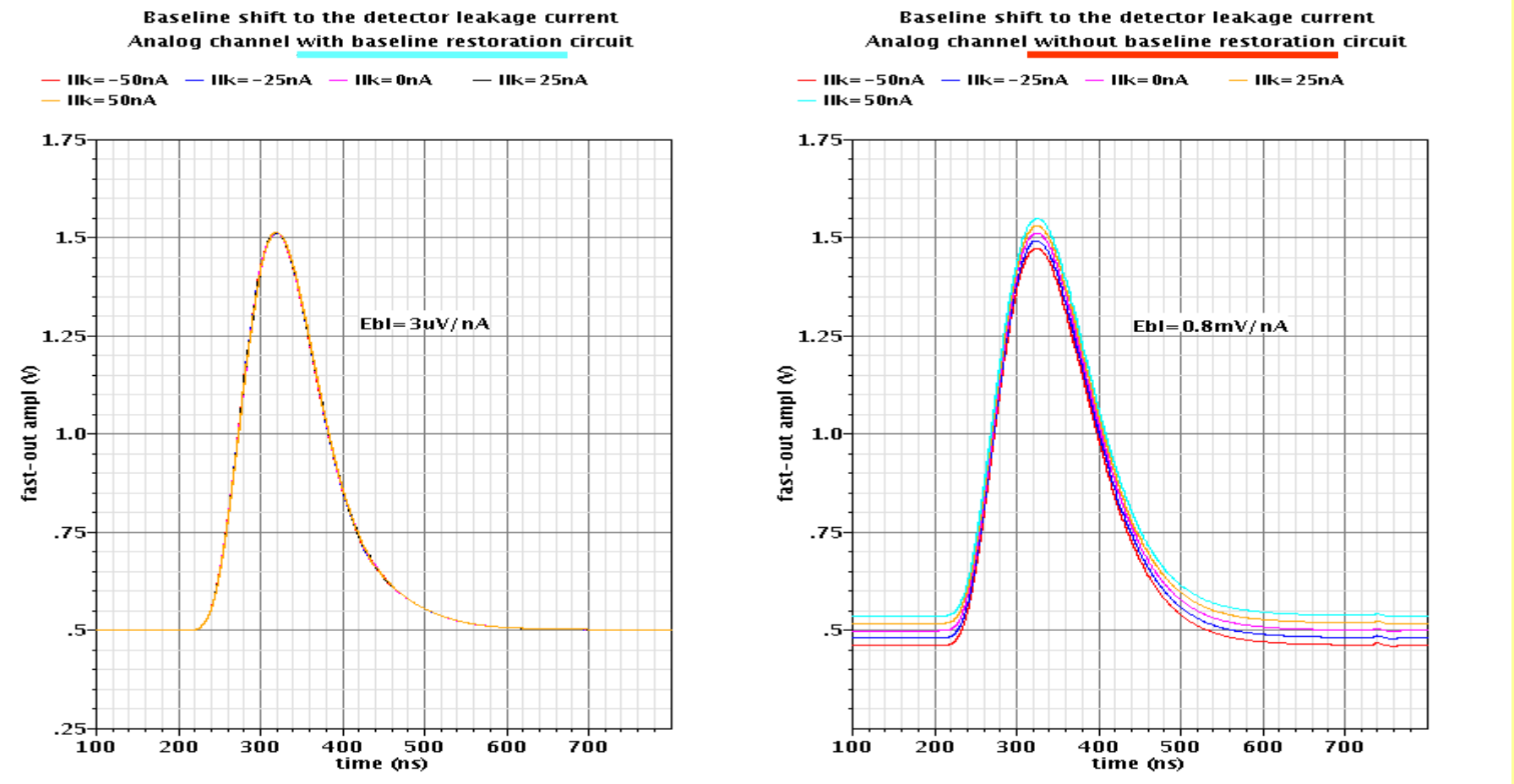
-short channel dead time even for large overload (ten times full range)
-very good double pulse separation and response to high pulse rate
-no base line perturbations

Channel response without fast recovery circuits:



-channel is dead for long time
-double pulse separation and response to high rate pulses are not possible
-important base line perturbations

3.4 Base line restoration due to detector leakage current and/or to high counting rate



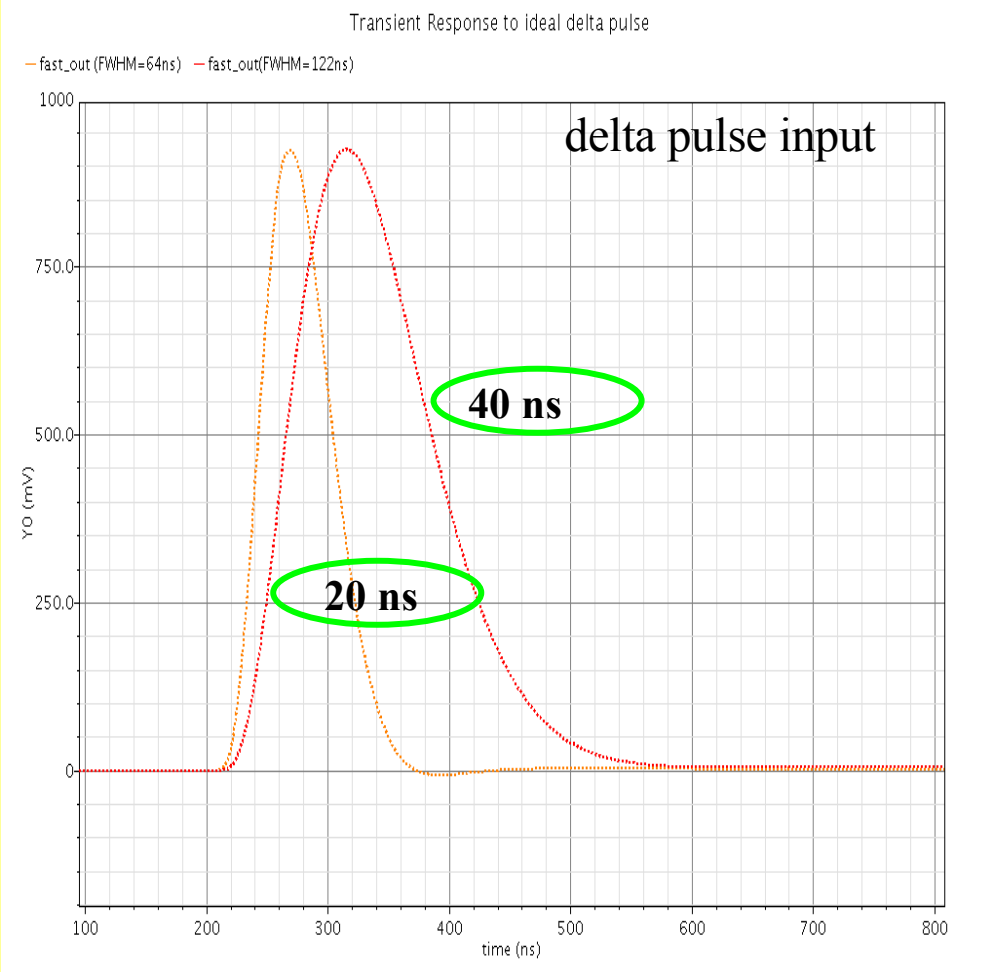
● ***Analog channel with base line restoration:***
- non significant base line shift

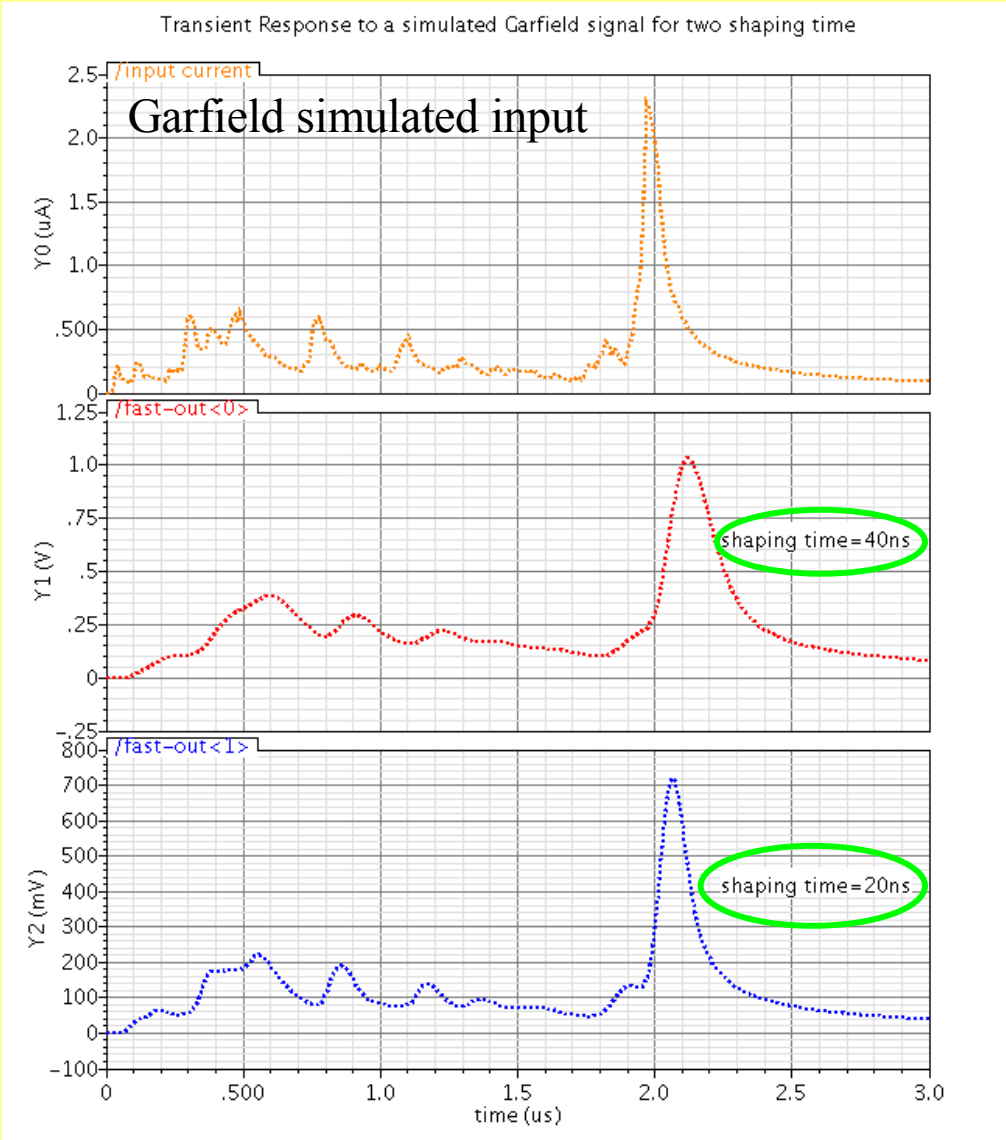
Ilk	DC(fast-out)
-50nA	499.8mV
-25nA	499.8mV
0nA	499.9mV
25nA	500.0mV
50nA	500.1mV

● ***Analog channel without base line restoration:***
- large base line shift

Ilk	DC(fast-out)
-50nA	461.3mV
-25nA	480.3mV
0nA	499.2mV
25nA	518.0mV
50nA	536.9mV

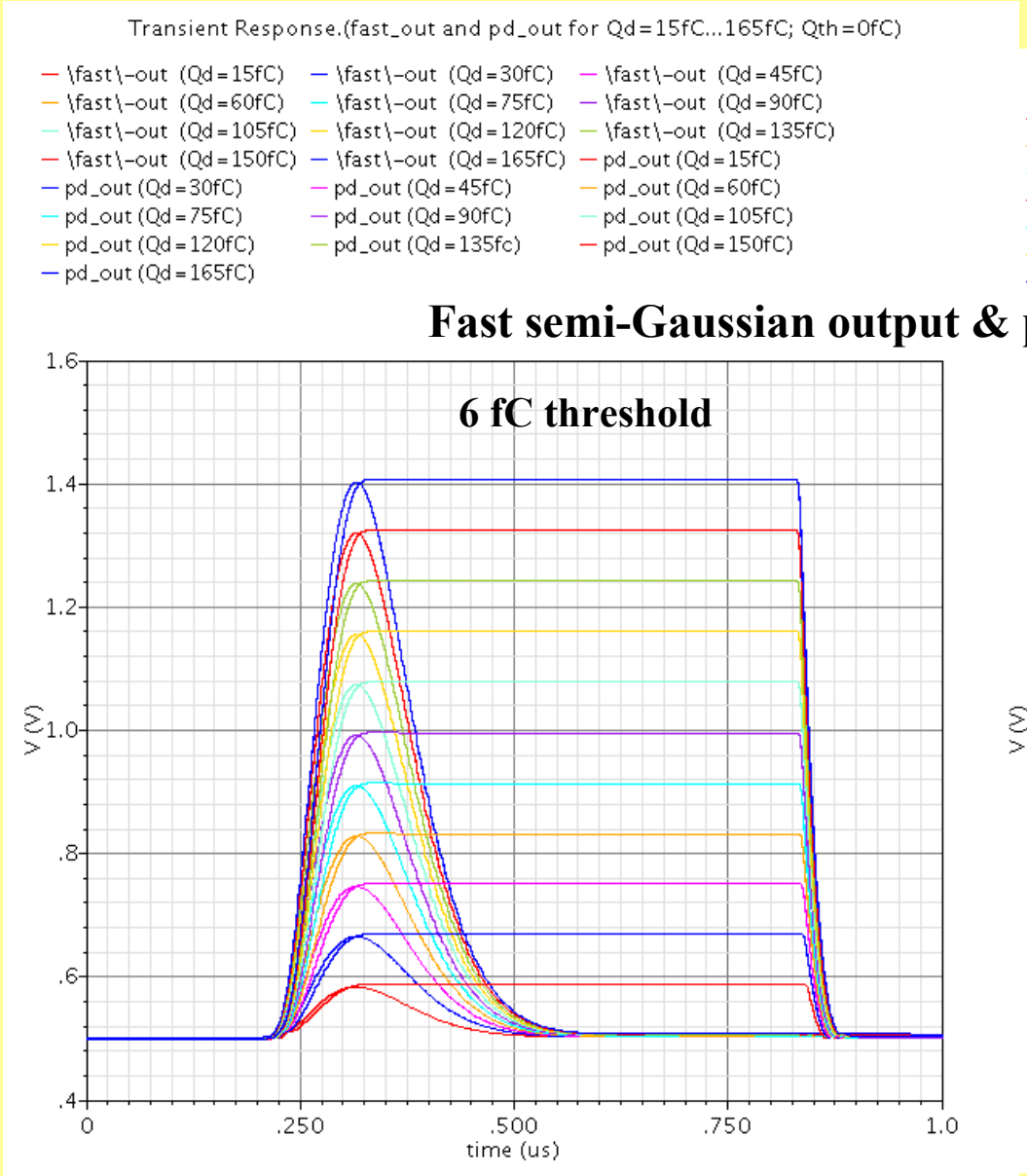
3.5 Shaping time selection

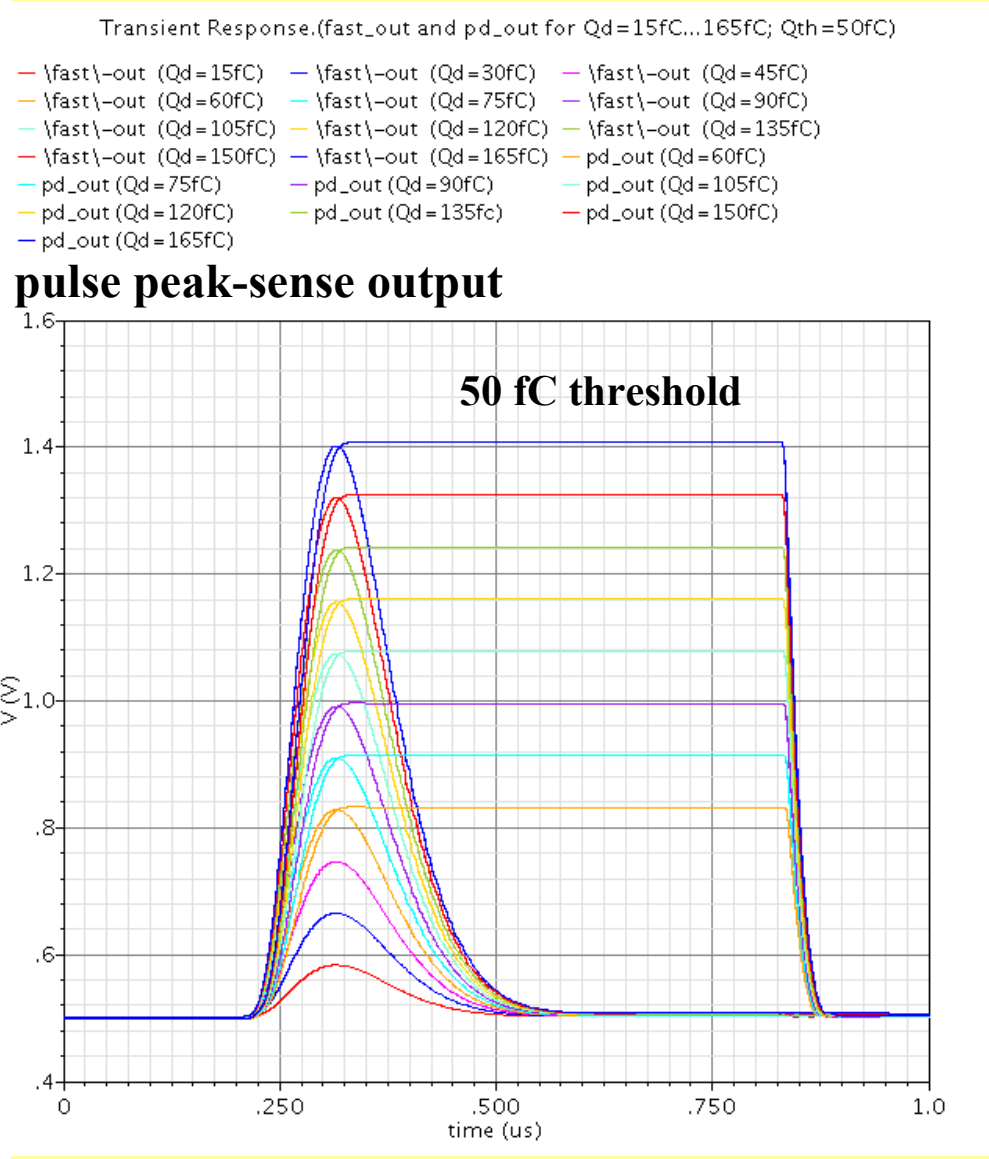




- logic level selection

3.6 Self trigger and pulse peak-sense circuits



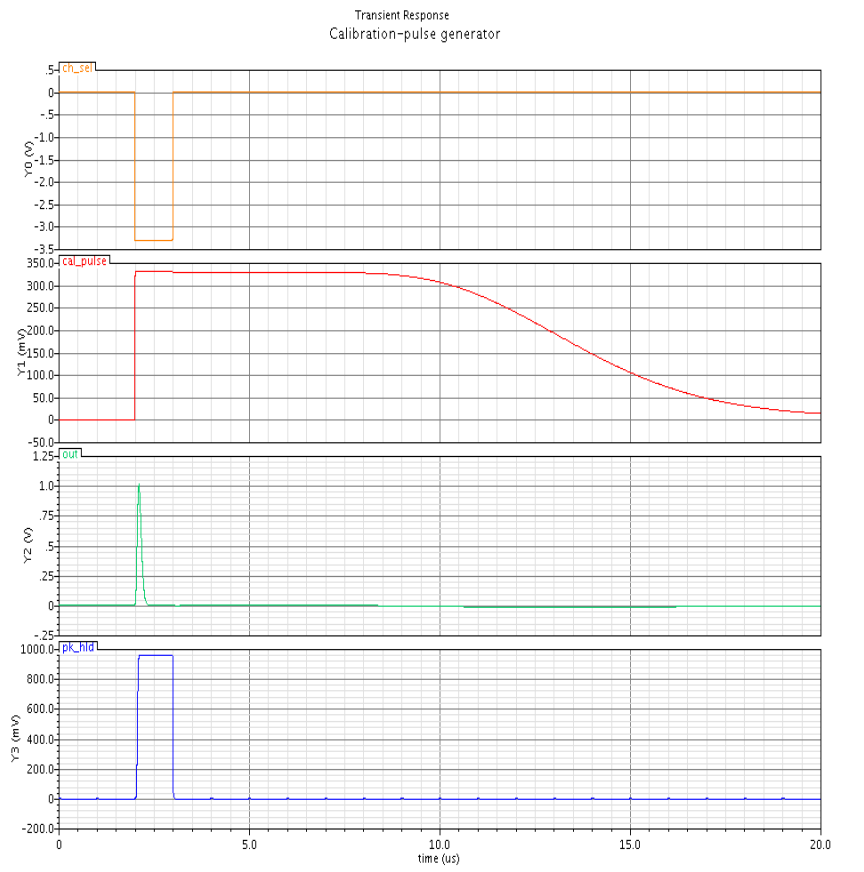


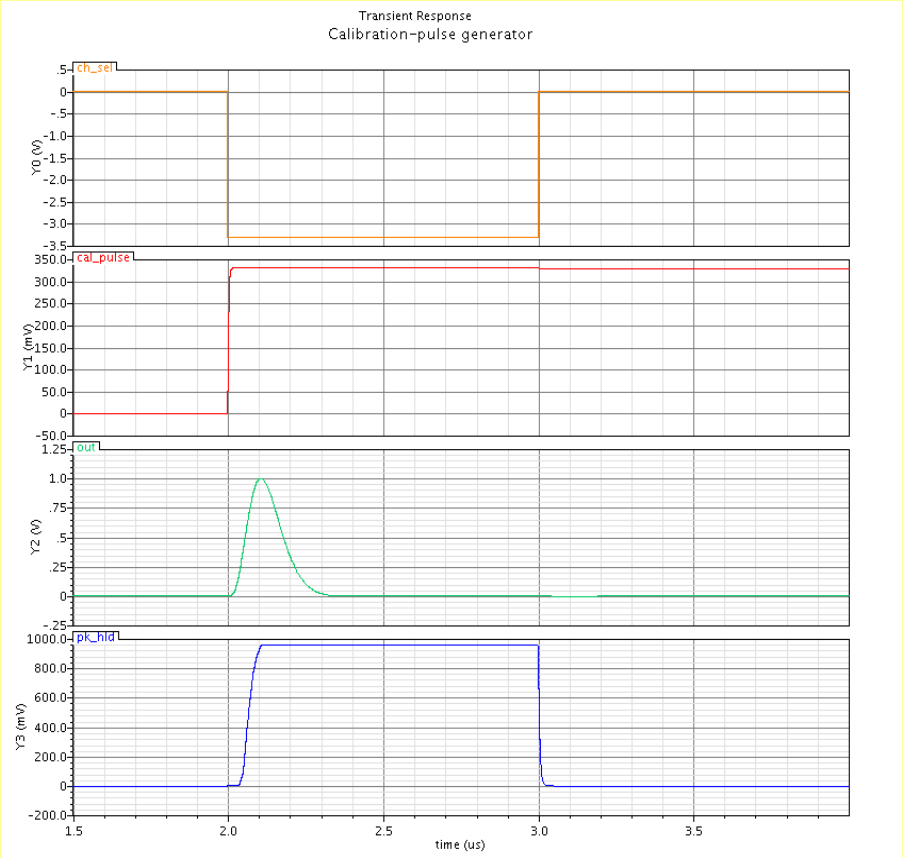
Fast semi-Gaussian output & pulse peak-sense output

- Self triggered (signal over the threshold)
- Variable threshold for selection of the useful amplitudes

4. Additional implemented circuits

4.1 Calibration pulse generator (improved version of the ALICE TRD)





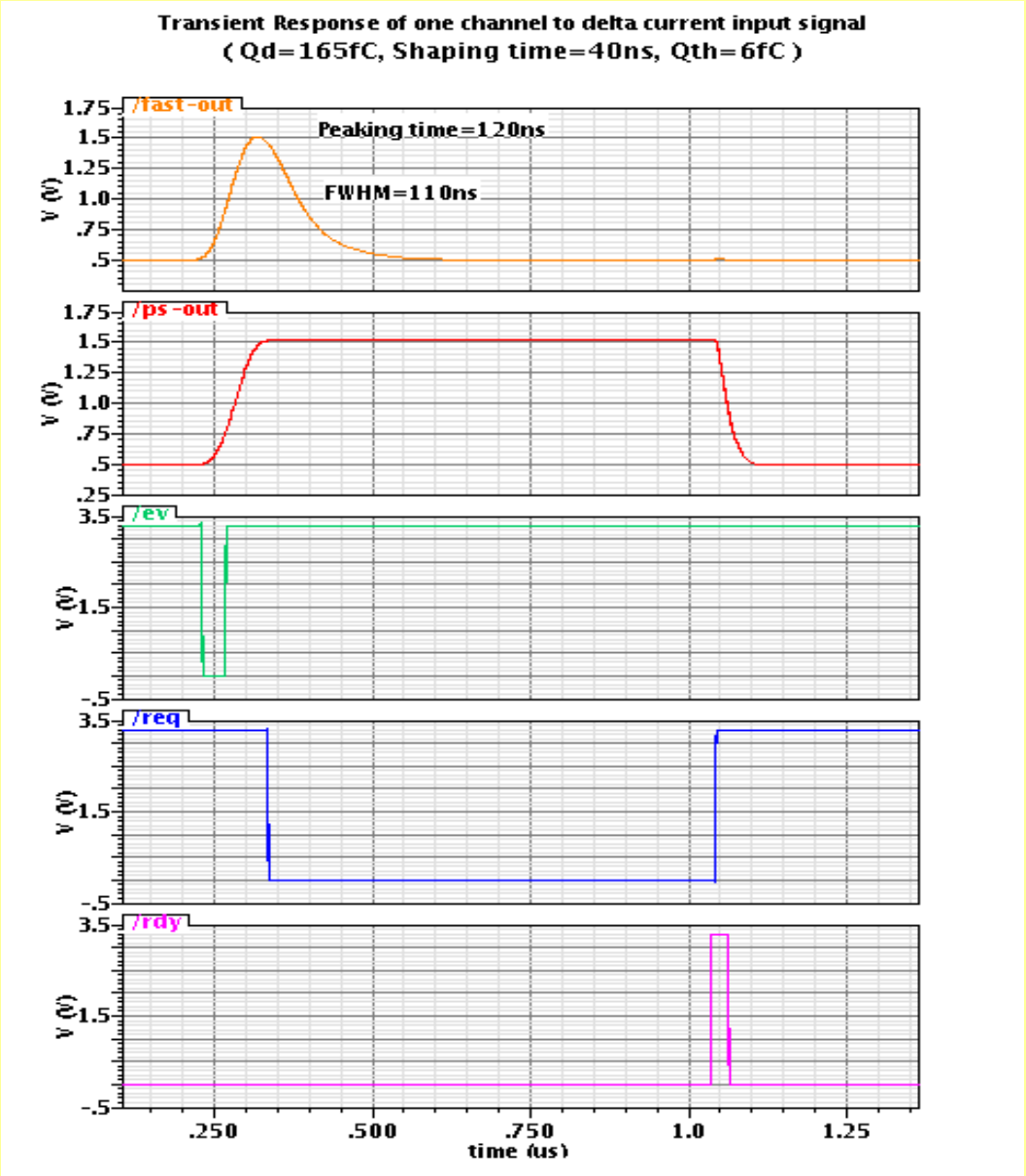
- Useful in finding channel gain
- No additional software needed for gain finding

4.2 Fast input/output interface for data processing

4.3 Reference and bias circuits

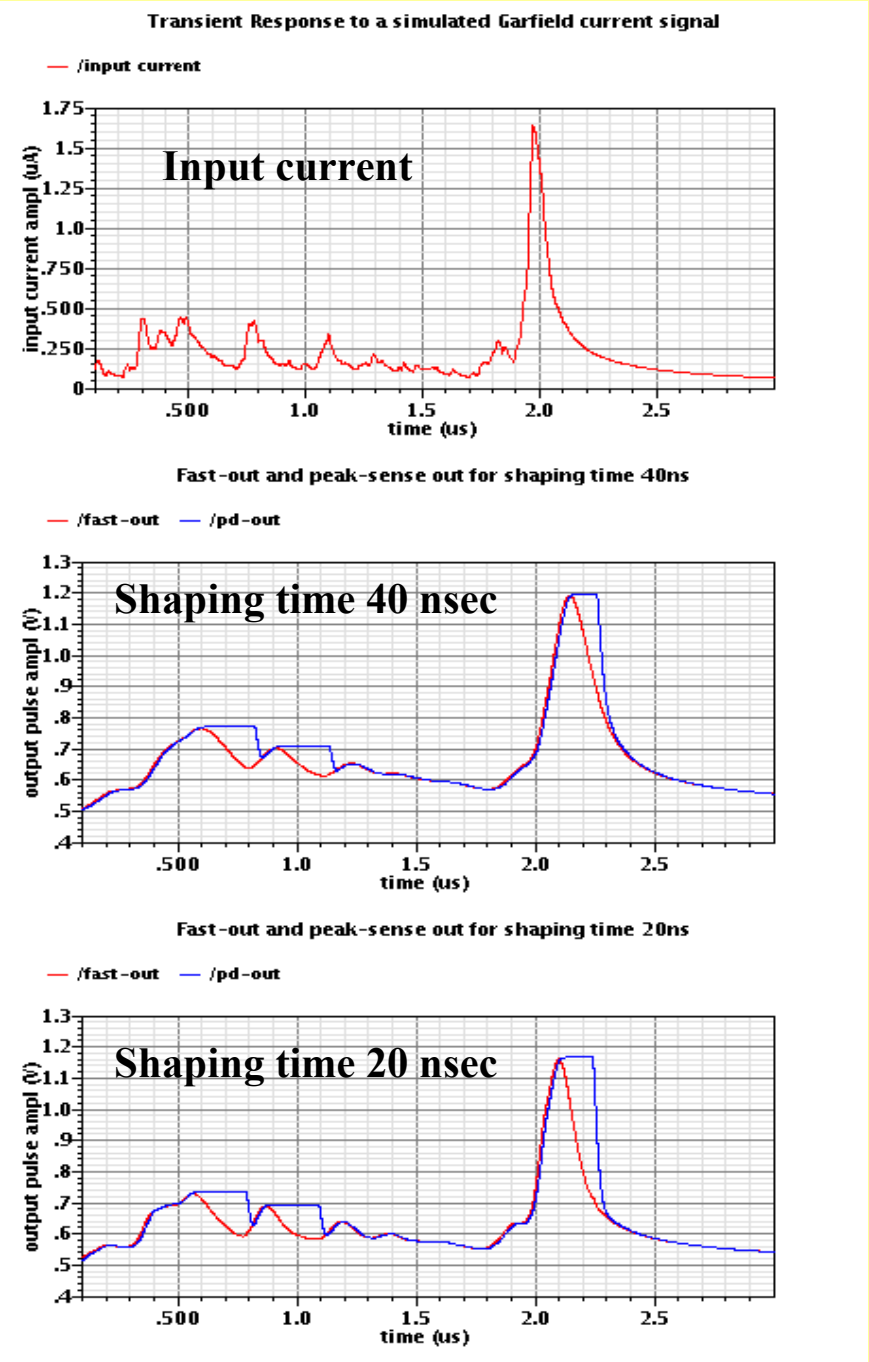
5. Main results

5.1 Typical response of one self triggered analog channel to delta current signal

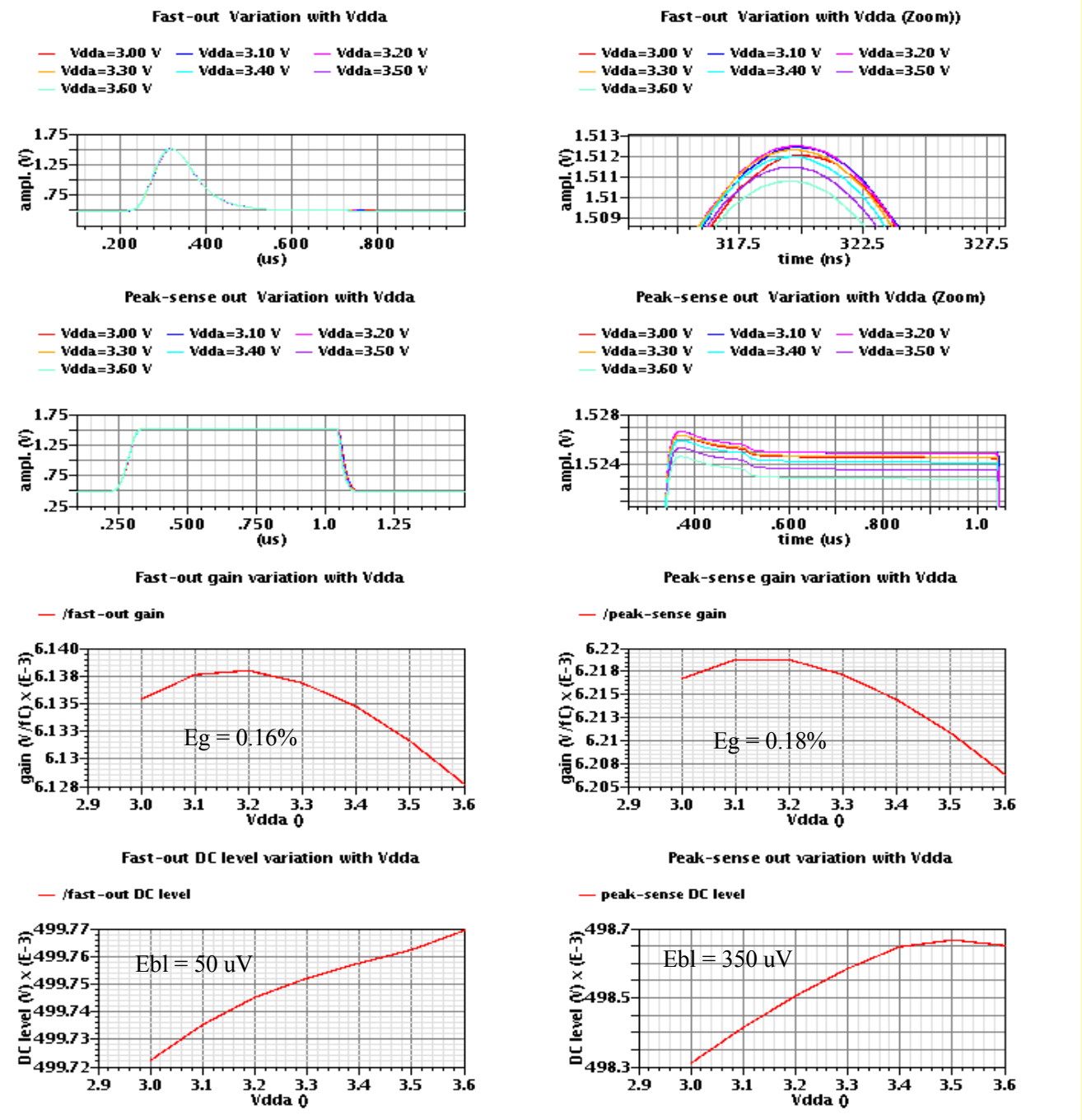


- Fast-out
- Peak-sense out
- Self trigger – event out
  - variable threshold (0...165fC)
  - logic levels
- Request
  -logic levels
- Ready
  -logic levels

5.2 Transient response to a simulated Garfield current signal



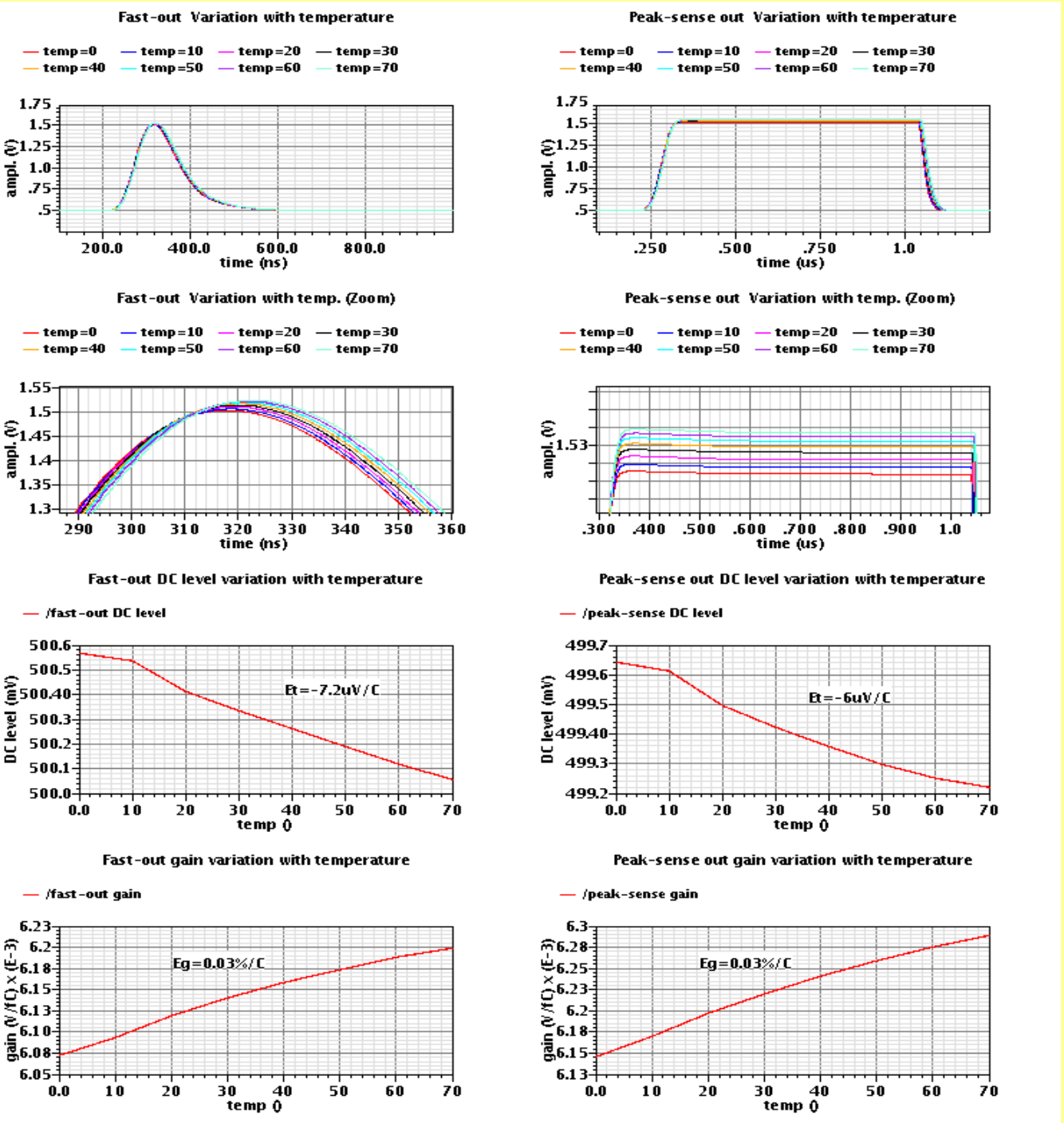
5.3 Fast-out and peak-sense out variations with voltage supply



- **Fast-out variations with Vdda=3V...3.6V**
  - gain variation < 0.16%
  - DC baseline variation < 50 µV

- **Peak-sense out variations with Vdda=3V...3.6V**
  - gain variation < 0.18%
  - DC baseline variation < 350 µV

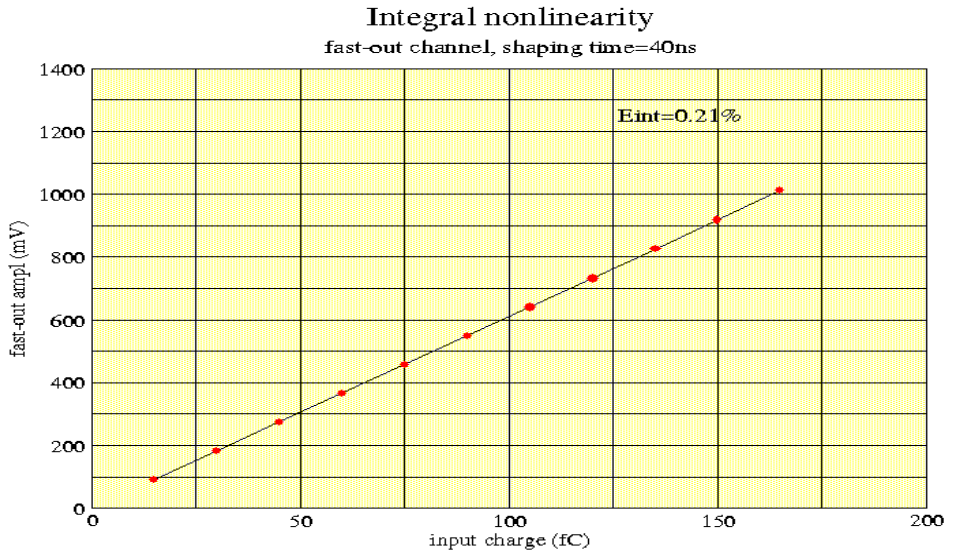
5.4 Fast-out and peak-sense out variations with temperature



- **Fast-out variations with temperature T=0° C...70° C**
  - gain variation <0.03%/ °C
  - DC level baseline variation <8µV/ °C

- **Peak-sense out variations with temperature T=0 C...70 C**
  - gain variation <0.03%/ °C
  - DC level baseline variation <6µV/ °C

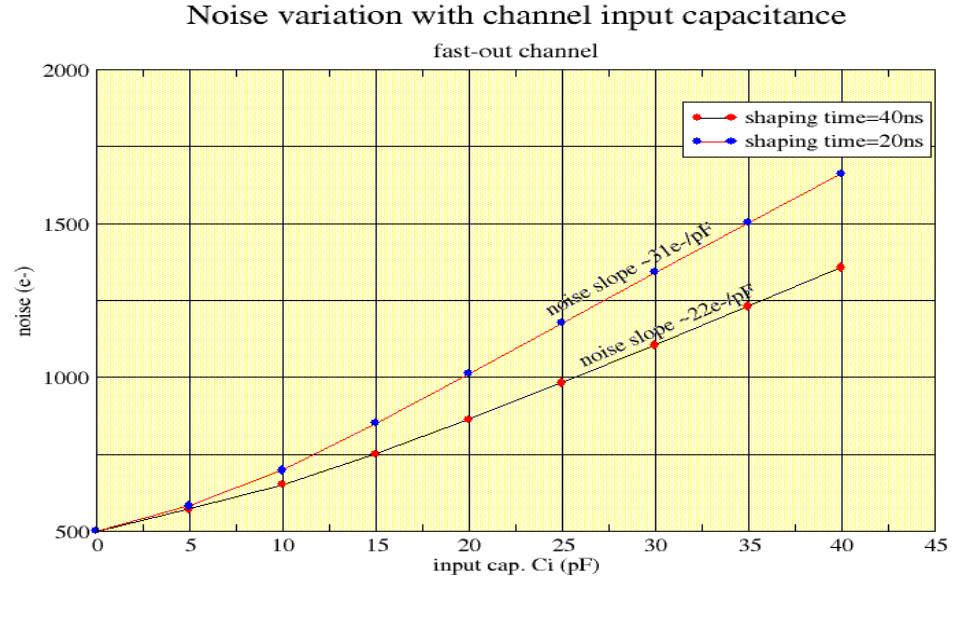
5.5 Integral nonlinearity specifications



- **Integral nonlinearity:**

-fast-out shaping time 20ns <0.47%
-fast-out shaping time 40ns <0.21%
-peak-sense out shaping time 20 ns <0.91%
-peak-sense out shaping time 40ns <0.19%

5.6 Noise specifications



- **Noise values for input capacitance Ci=25 pF**:

- 980 electrons for shaping time 40 ns
- 1170 electrons for shaping time 20 ns

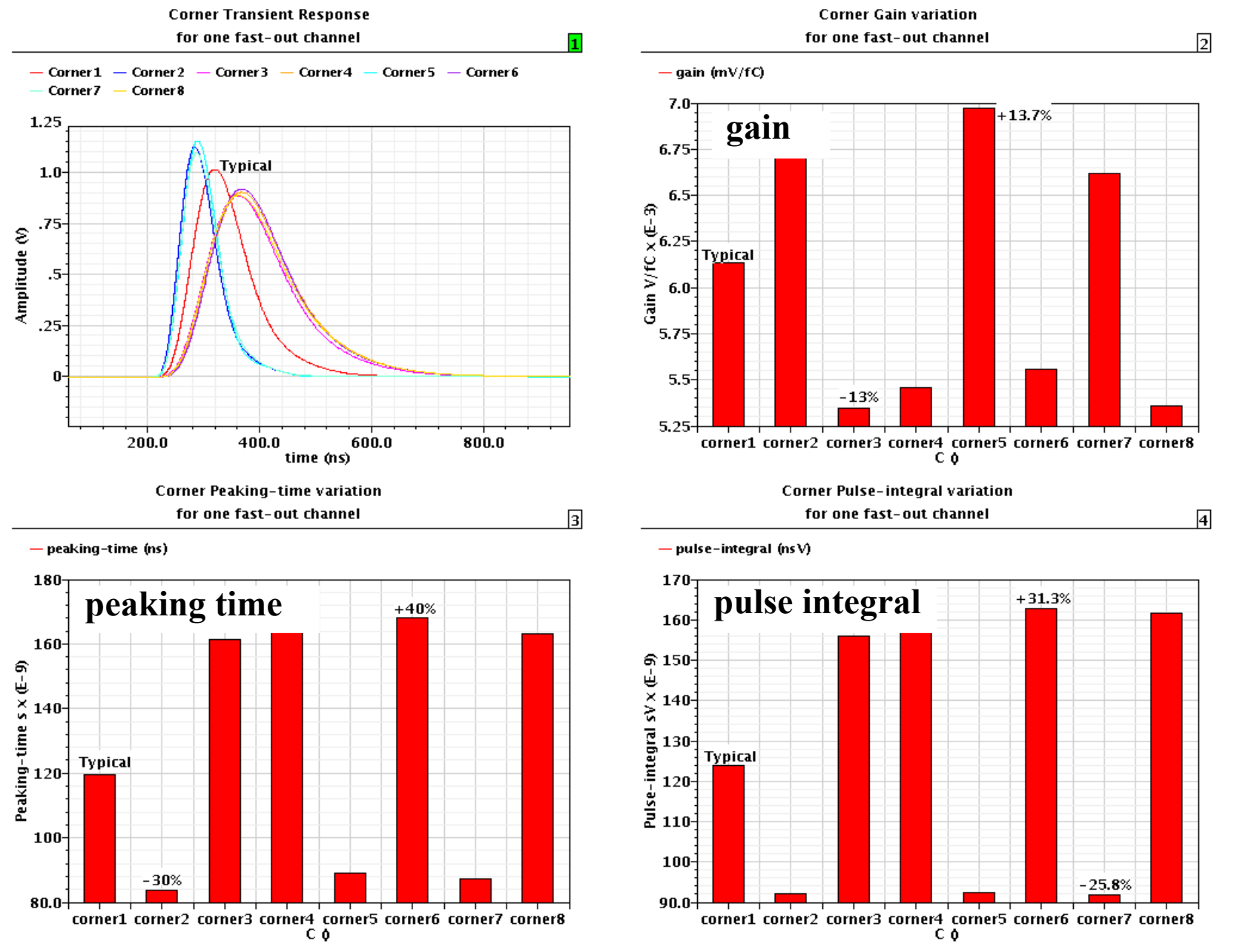
- **Noise slope for Ci=10pF...40pF**

- about 22 electrons/pF for shaping time 40ns
- about 31 electrons/pF for shaping time 20ns

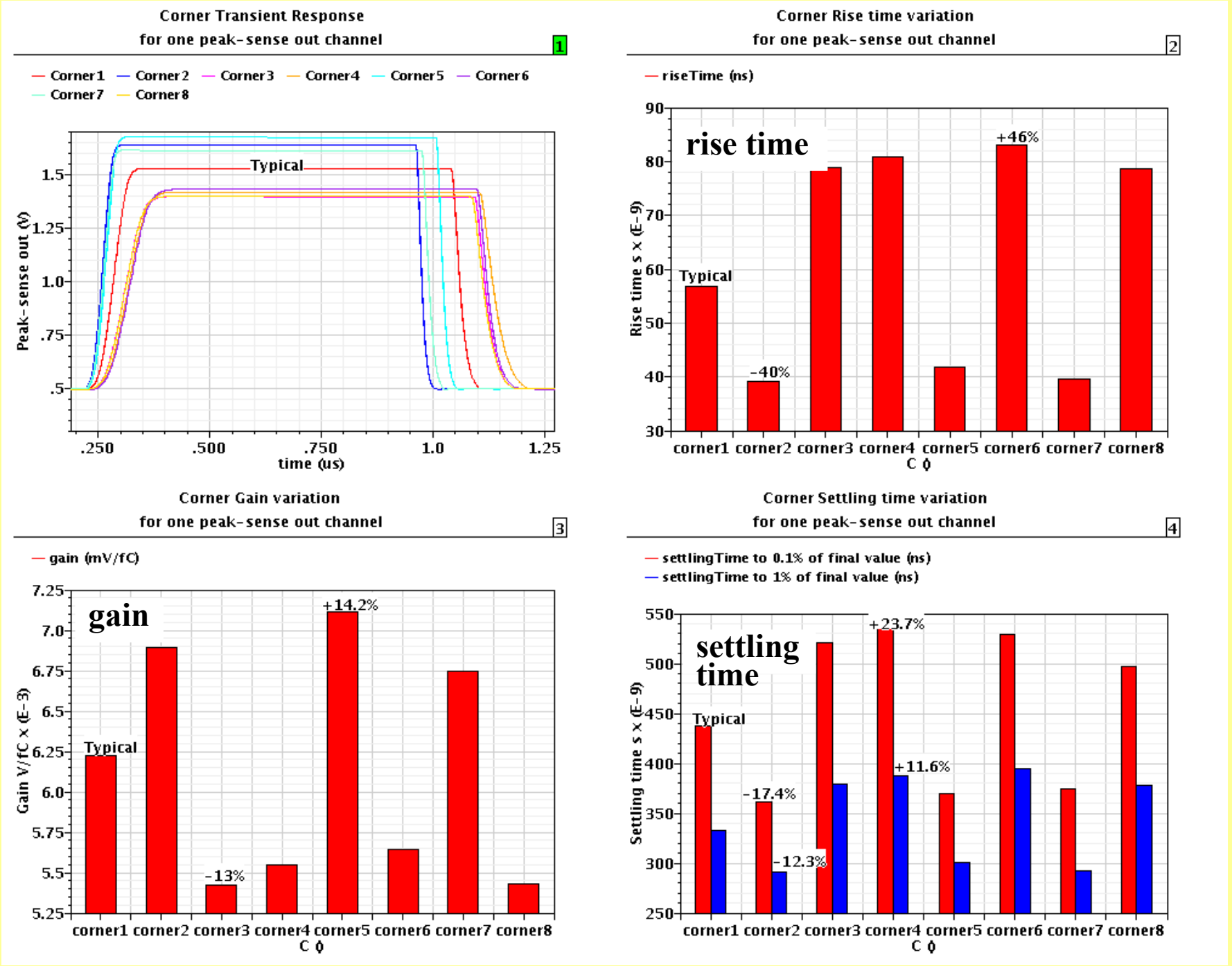
5.7 Corner specifications *(Foundry mandatory "Corner analysis")*

Corner parameters: wp,ws,wPth, wNth, T=0°…70°C, Vd=3.0 … 3.6V

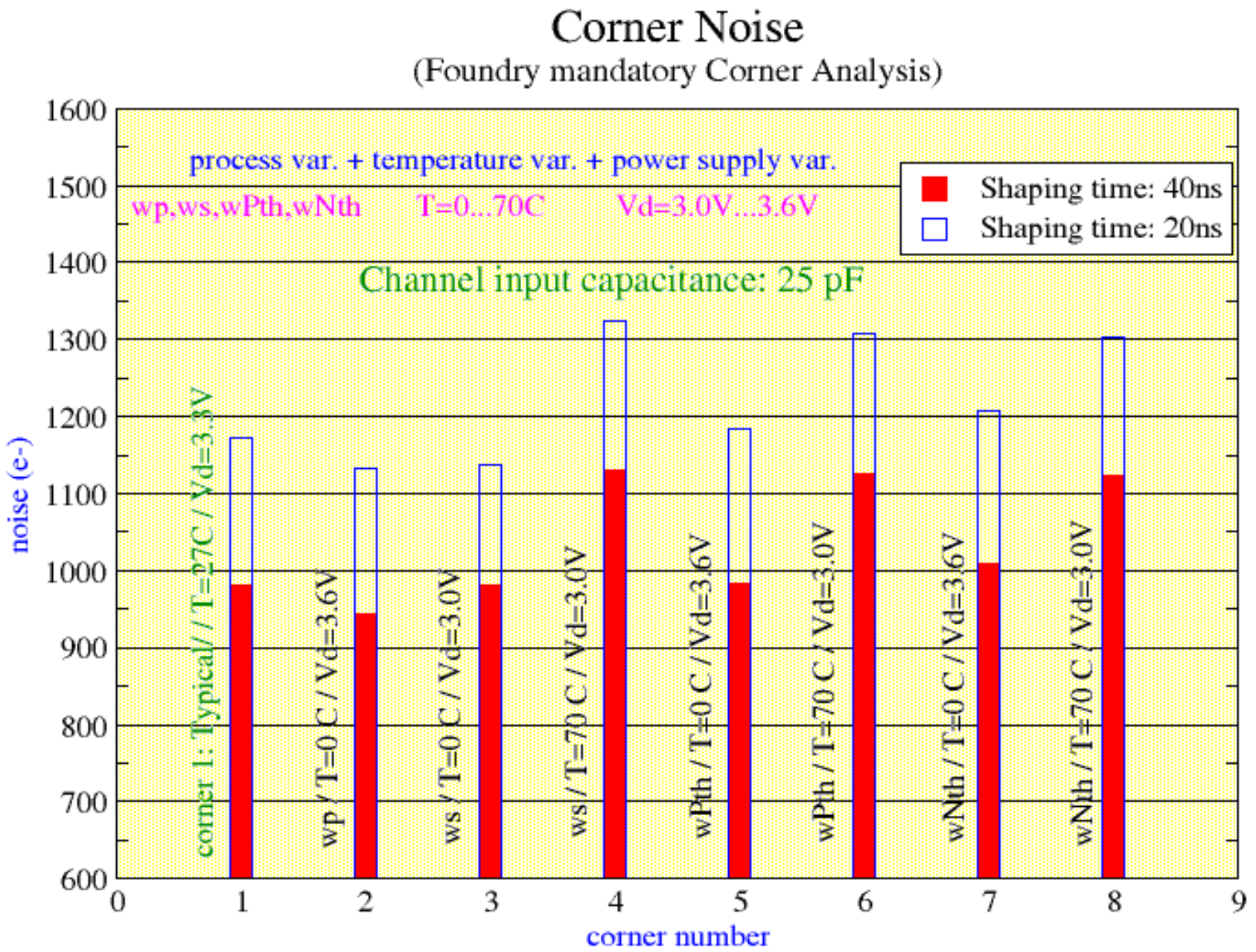
5.7.1 Fast-out:



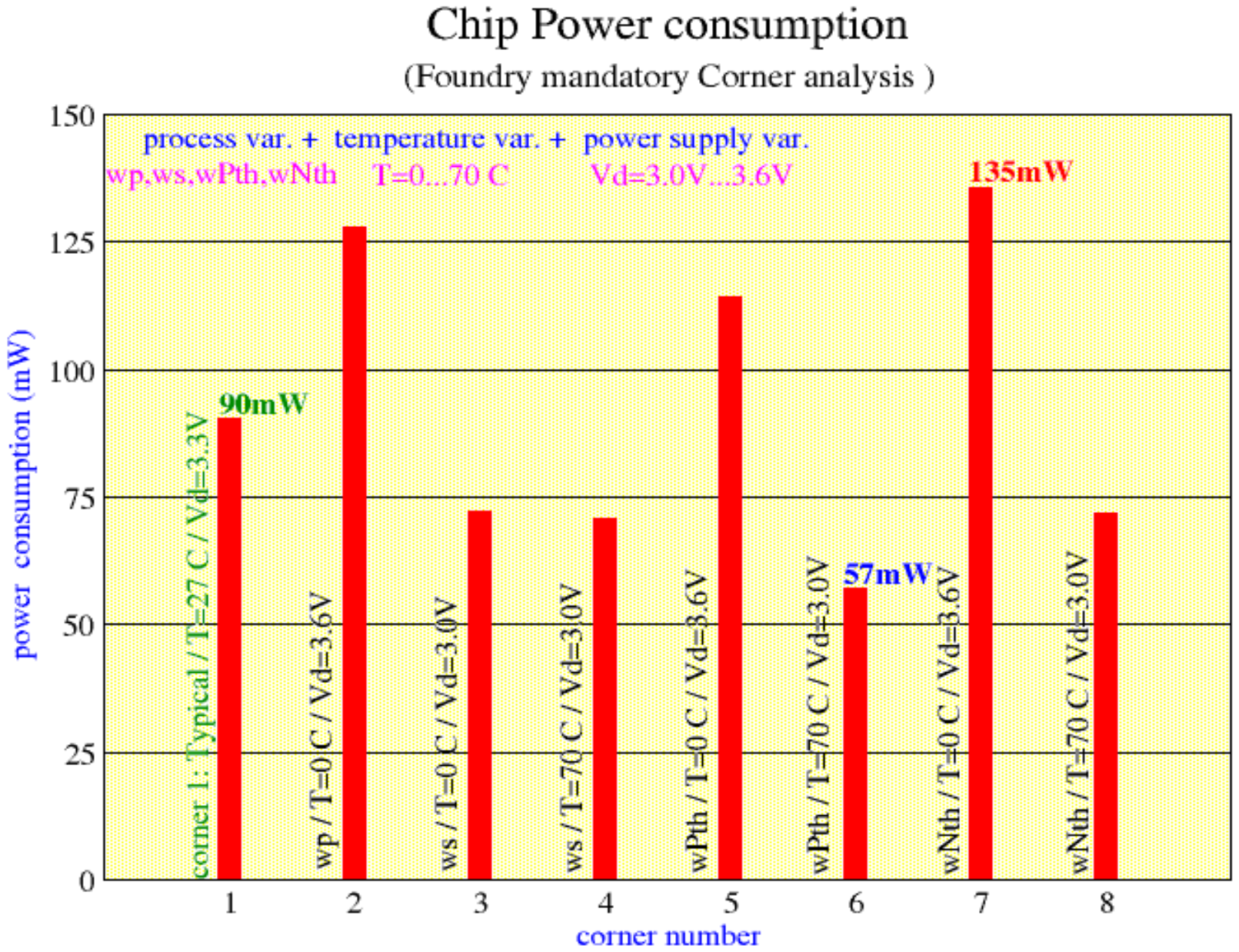
5.7.2 Peak-sense out:



5.7.3 Noise variation in corners

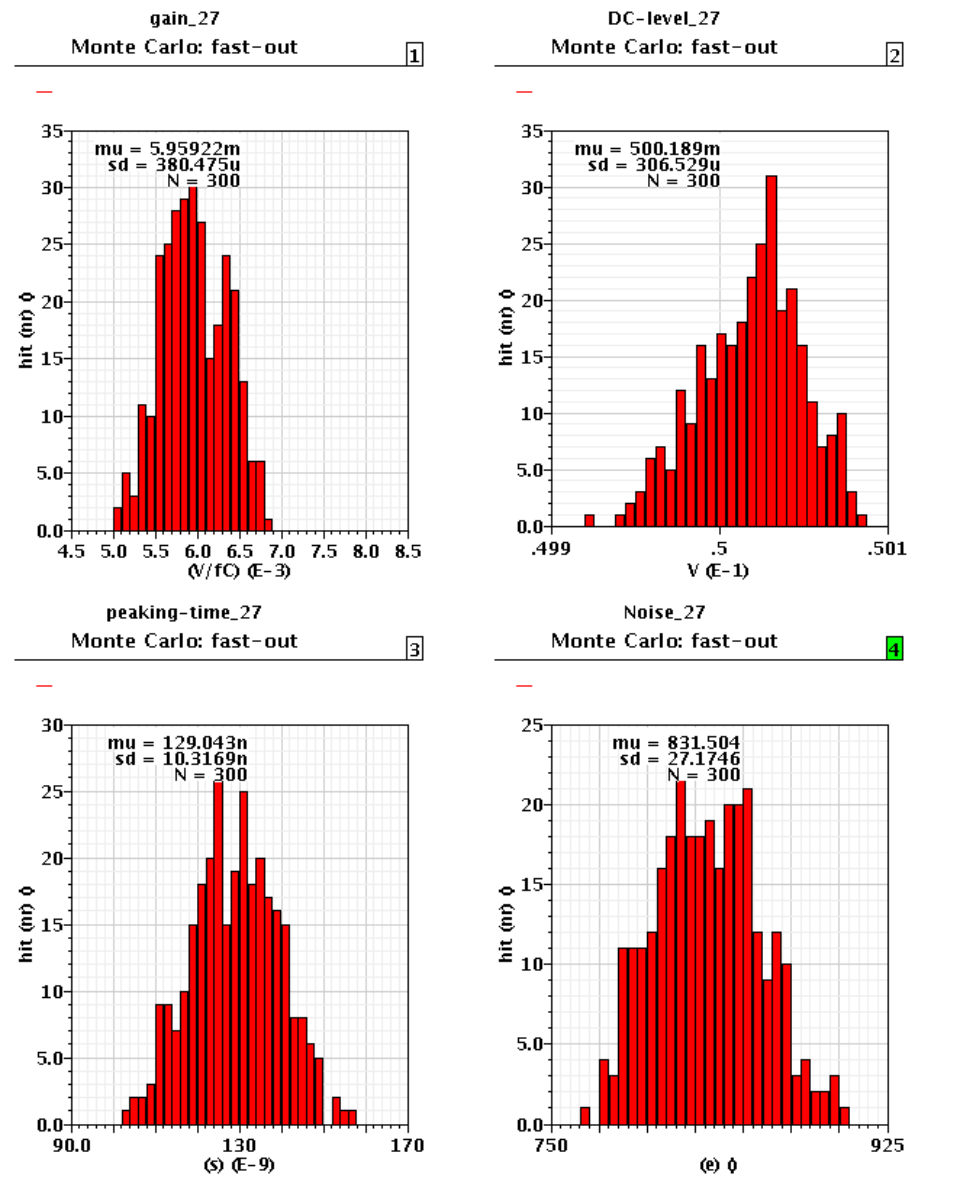


5.7.4 Chip power consumption in corners

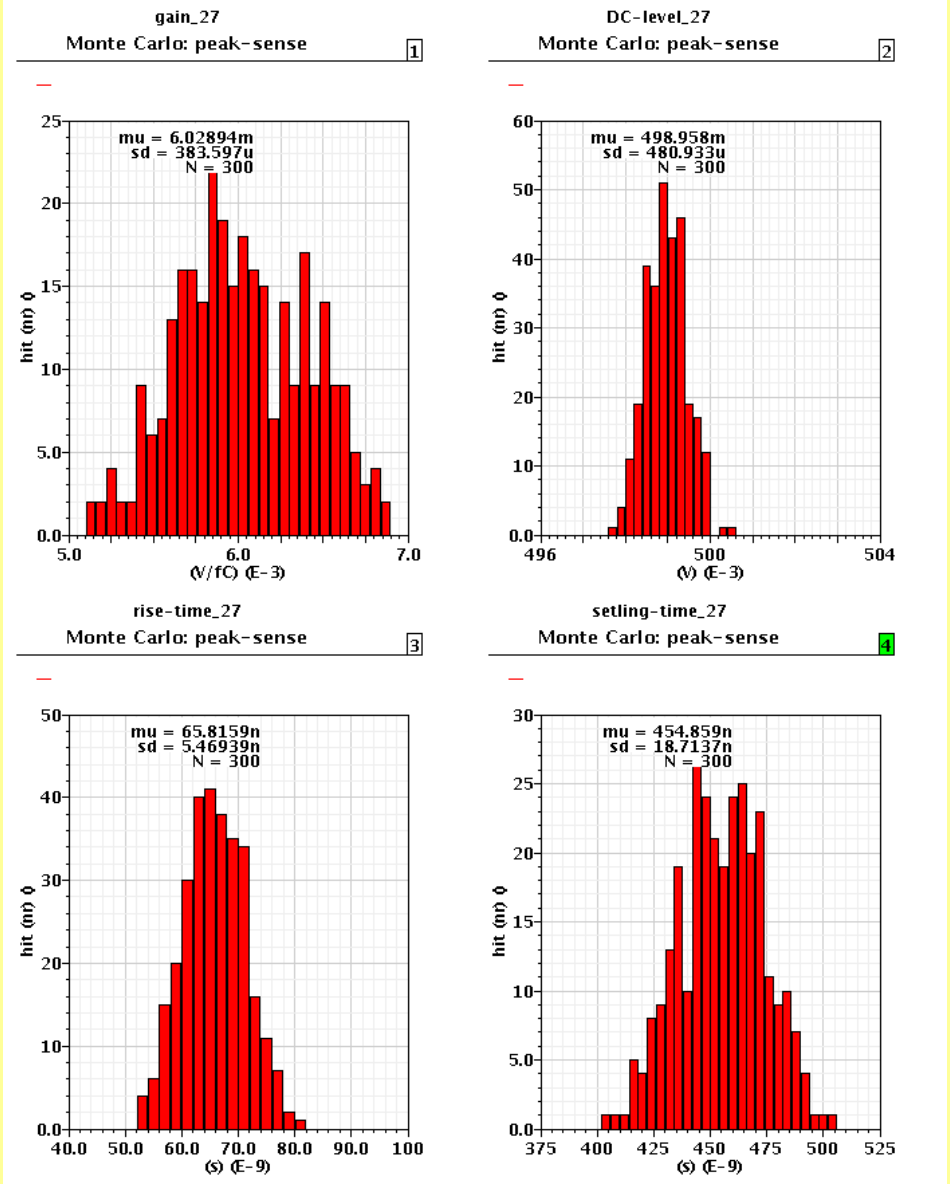


5.8 *Monte Carlo analysis*

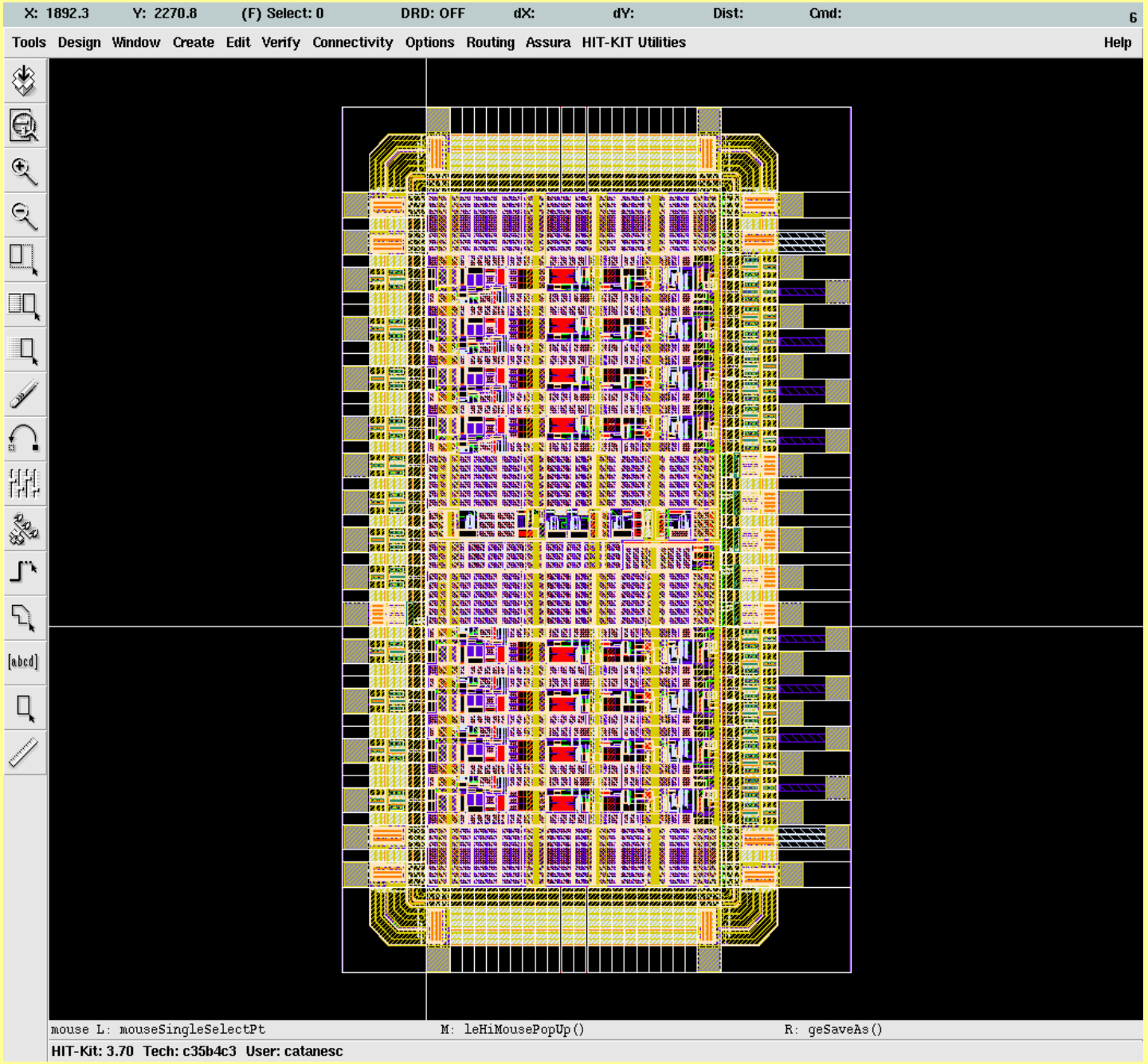
5.8.1 Fast-out:



5.8.2 Peak-sense out:



6.Layout of the first version of NIPNE analog chip for HCR TRD



7. Conclusions

Main desirable features were implemented to the chip:

- Good response to double pulse
- Good response to high pulse rate
- Fast recovery from overload
- Stable baseline to leakage current, temperature and voltage supplies variations
- More analog signal processing and peak-sense output facility
- Self triggered channel capability
- Input/Output interface
- Robust design
- First version of NIPNE chip for high counting rate TRD was submitted last November, already delivered, the bonding was done, preliminary tests performed
- Two FEE boards were done for tests and data acquisitions

Special thanks to Volker Lindenstruth and Ralf Achenbach

for their support in bonding the first CHIPs @ KIP